CMOS Logic style / CMOS Schematic:-

Q) Draw the CMOS schematic of (i) 3 i/p NOR gate
(ii) $Y = AB+CD$.
(iii) AOI logic
(iv) OAI logic.
(v) 2 i/p XOR gate.
(vi) $Y = \overline{A(B+C)+DE}$

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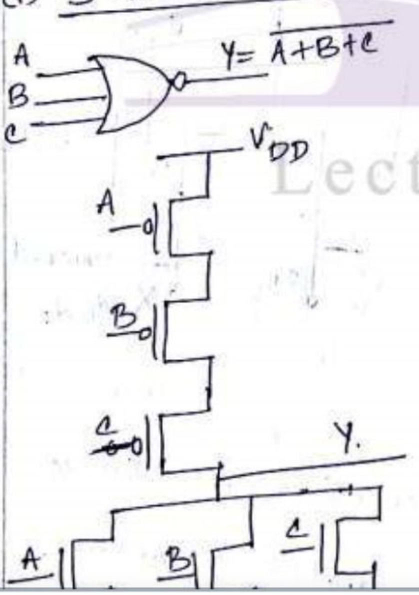
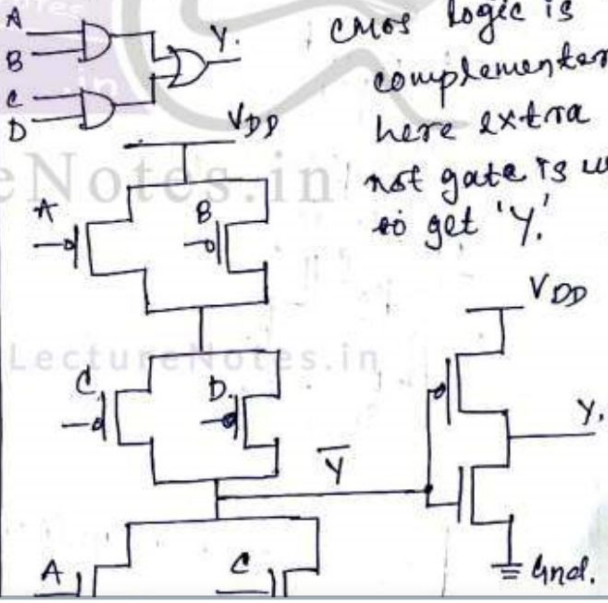
Note

'·' (multiplication) operation	'+' (addition/OR) operation.
→ PMOS connected in parallel. → NMOS connected in series	→ PMOS connection in series → NMOS connected in parallel.

(i) 3 i/p NOR gate


A
B
C
$Y = \overline{A+B+C}$
V_{DD}
A
B
C
Y.
A
B
C

(ii) $Y = AB+CD$.


A
B
C
D
Y.
V_{DD}
A
B
C
D
$\overline{Y}$
V_{DD}
Y.
Gnd.
A
C

Note
As always o/p of CMOS logic is complementary here extra not gate is used to get 'Y'.

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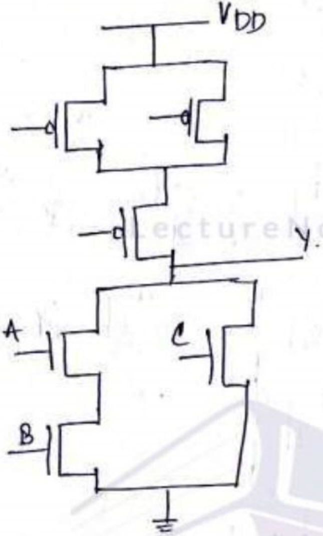
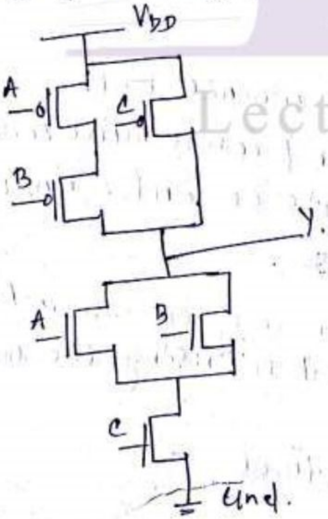
(iii) AOI Logic (AND-OR-Invert) logic:-

Here 3 i/p AOI Logic. $Y = \overline{AB+C}$

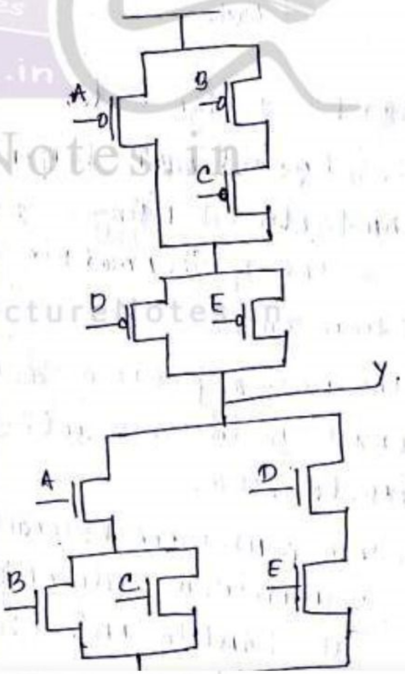


(iv) OAI (OR-And-Invert) Logic

3 i/p OAI logic $Y=\overline{(A+B)\cdot C}$

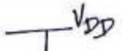

VDD
A
C
B
Y.
A
B
C
Gnd.

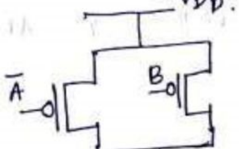
(vi) $Y=\overline{A(B+C)+DE}$

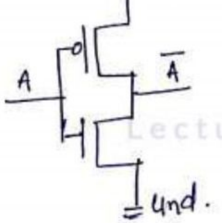

A
B
C
D
E
Y.
A
D
B
C
E

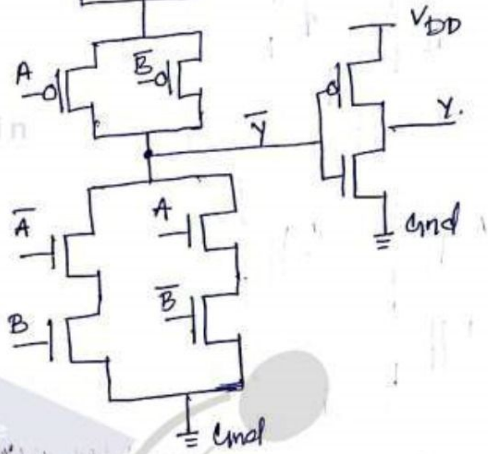
(v) 2 i/p XOR gate.

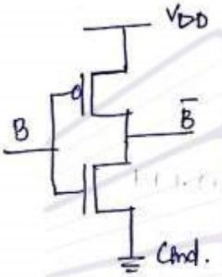
$Y=\bar{A}B+A\bar{B}$








V_DD
A
B̄
Ȳ
Y.
Gnd
Ā
A
B
B̄
Gnd



MOSFET Design Rule:-

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, known as design rule.

→ The main objective of design rule is to achieve a high overall yield and reliability while using the smallest possible area.

→ Design rules are basically of 2 types

(I) Micron rule (μ)
(II) Lambda rule (λ)

(I) Micron rule (μ):- In which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

(II) Lambda rule (λ) :- which specify the layout constraint in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometric constraints.

→ Design rules are the interface between circuit designer and process engineer.

→ Layout Design rule checker (DRC) automatically verifies that no design rules have been broken.

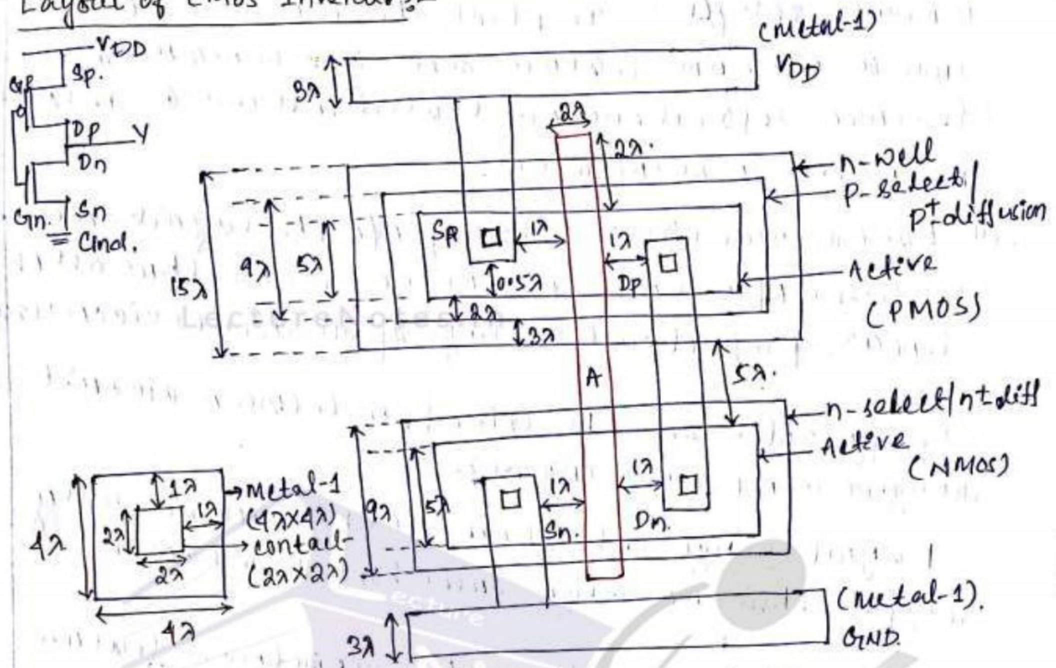
Lambda(λ) → Distance by which a geometrical feature of any one layer may stay from any other geometrical feature on the same layer or any other layer.

→ λ used to prevent IC ~~a~~ manufacturing problems due to mask misalignment or exposure and development variations on every feature, which otherwise could lead to

- over-diffusion
- over etching
- inadvertent transistor creation etc.

→ 'λ' is the minimum dimension which can be accurately reproduced on the silicon wafer for a particular technology.

Layout of CMOS Inverter:-


VDD
Sp.
Gp
Dp
Y
Dn
Gn.
Sn
Gnd.
(metal-1)
VDD
3λ
2λ
2λ.
n-well
p-select/ p+ diffusion
Active (PMOS)
Sp
1λ
1λ
Dp
0.5λ
2λ
3λ
15λ
9λ
5λ
A
5λ.
n-select/n+ diff
Active (NMOS)
9λ
5λ
1λ
1λ
Sn.
Dn.
1λ
1λ
2λ
2λ
4λ
4λ
Metal-1 (4λ×4λ)
contact (2λ×2λ)
(metal-1).
GND
3λ

p-well → Yellow
N-well → Green.
Metal-1 → Blue.

contacts → Black.
Active → Green.
p-select → yellow.

n-select → Green.

Lay out of 2-i/p NAND gate:-

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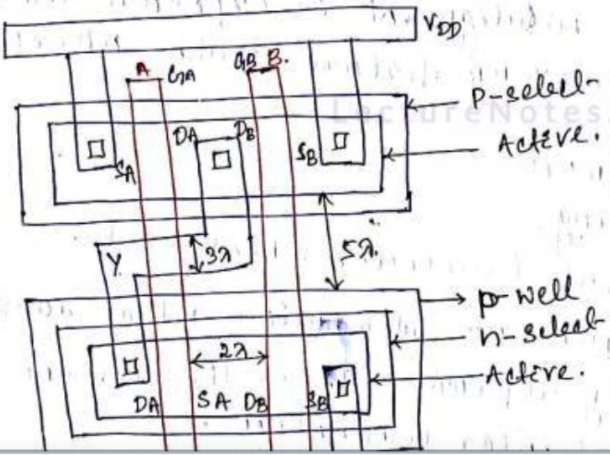
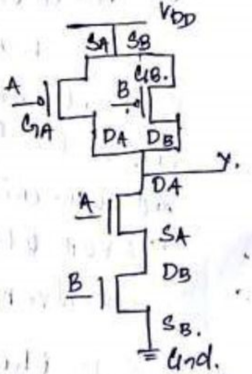

VDD
A
GA
GB
B.
p-select
Active.
DA
DB
SA
SB
Y
3λ
5λ
p-well
n-select
2λ
Active.
DA
SA
DB
SB


VDD
SA
SB
GB.
A
GA
B
DA
DB
Y.
DA
A
SA
DB
B
SB.
Gnd.

SA → Source of A
DA → Drain of A