82C54 Programmable Timers/ Counters

Counter & Timer

- 82C54 is an IC used as a counter or timer.

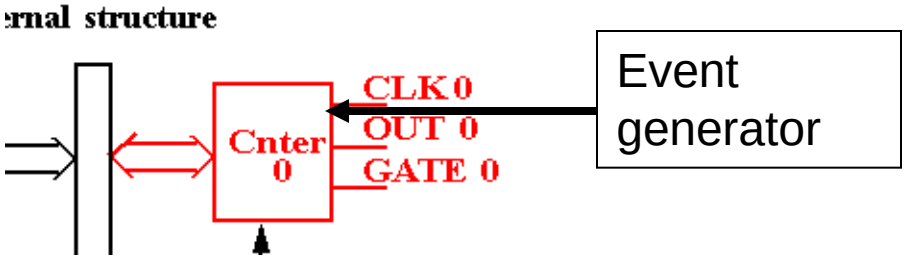
1. **Counter**: it counts the events.

The pulses generated by the occurrence of event are connected at its CLK input & the counter counts them. The events may be periodic or A-periodic.

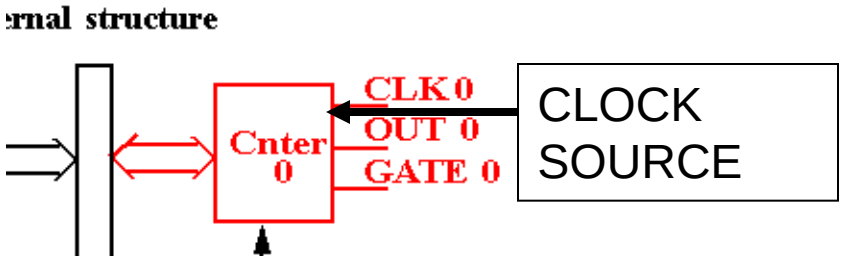
2. **Timer:** It is used to produce delays between two Events.

The pulses generated by the periodic clock source are connected at its CLK input & the timer counts them.

Counter & Timer



Counter



Timer

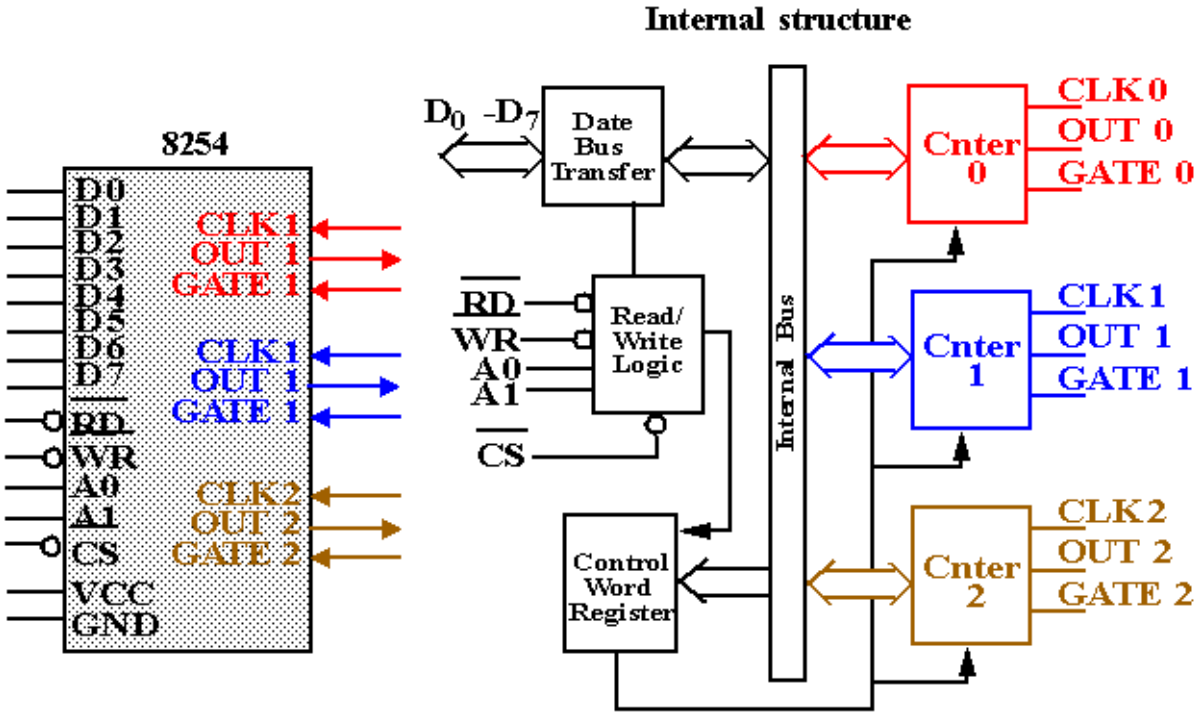
Hardware delays

- Delays or event counting can be done by software instructions but µP would be busy in running the delay sub routines & can't do any thing else.
- The hardware timers/counters relieve the processor by doing this task itself & interrupting the processor when the required delay or counting is completed.

82C54

- 3 sixteen bit counters, only counting down e.g. 10, 9, 8,7,……
- CLK (clock) The counter counts the pulses connected with the CLK input.
- GATE: high on gate will start the counter & low will stop the counter.
- OUT: give a pulse or square wave at output.

Programmable Timer 8254



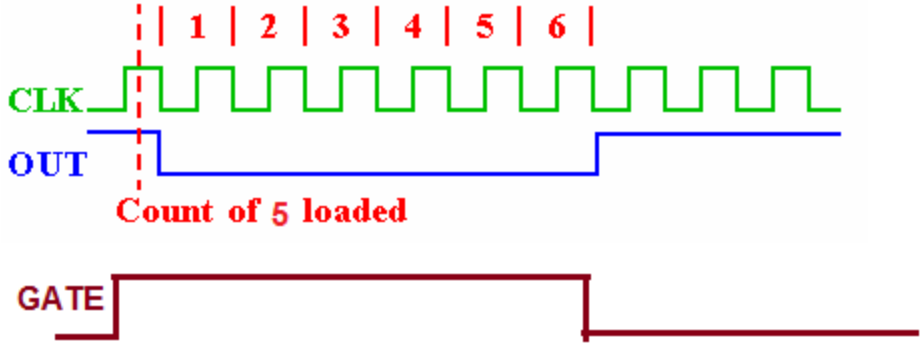
A_1	A_0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word

Modes of Operation

Interrupt on terminal count (mode 0)

(Initial value N=5)

After (N+1 =6) pulses the counter decrements to zero & sends high on OUTPUT. During 6 pulses the GATE should be high, if it goes low, the counting will be stopped till it becomes high again. However the counting will resume from the same point where it was stopped.

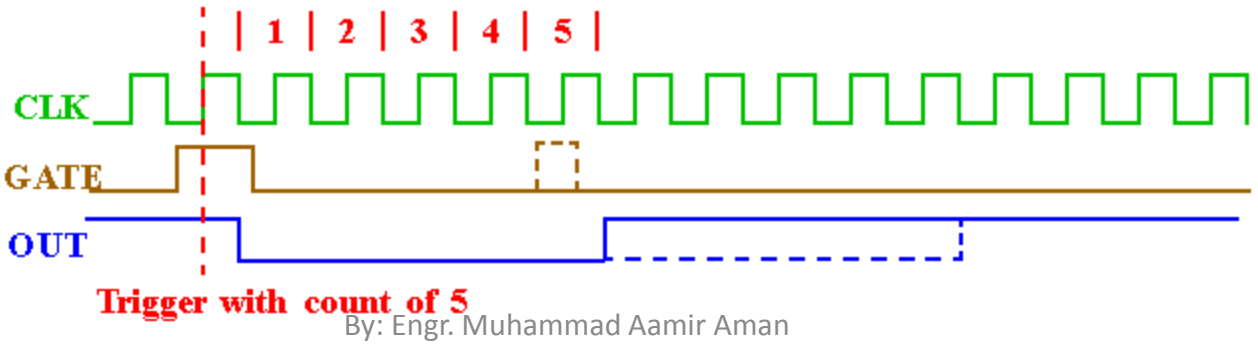


Modes of Operation

Programmable One shot (mode 1)

(Initial value N= 5)

After (N =5) pulses the counter decrements to zero & sends high on OUTPUT. A high pulse is only required on GATE just to start counting (trigger), if during counting another trigger occurs at GATE, the counting will restart from initial count (N=5).

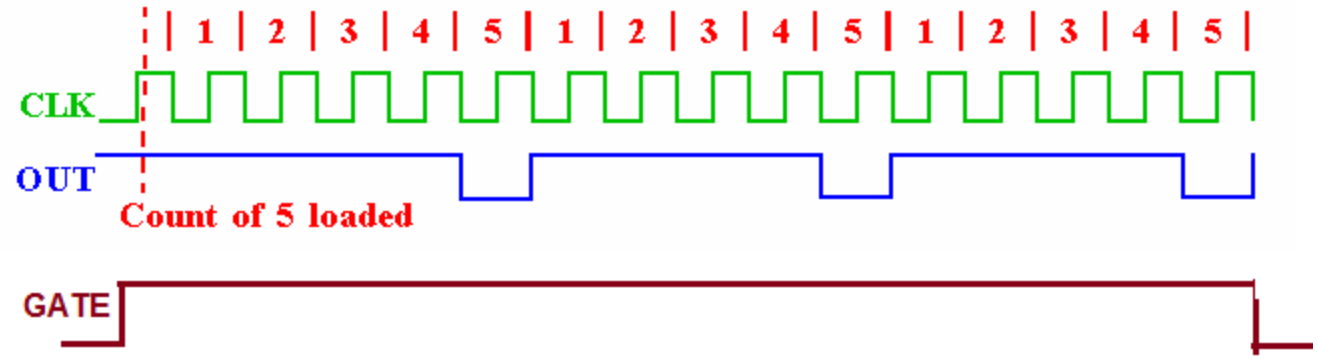


Modes of Operation

Rate generator (mode 2)

(Initial value N= 5)

It divides the input clock frequency by N. When the counting starts, OUTPUT becomes high. After 4 pulses, the Output goes low for 1 clock period So for N clock cycles, 1 output cycle is generated. Gate must remain high during counting.

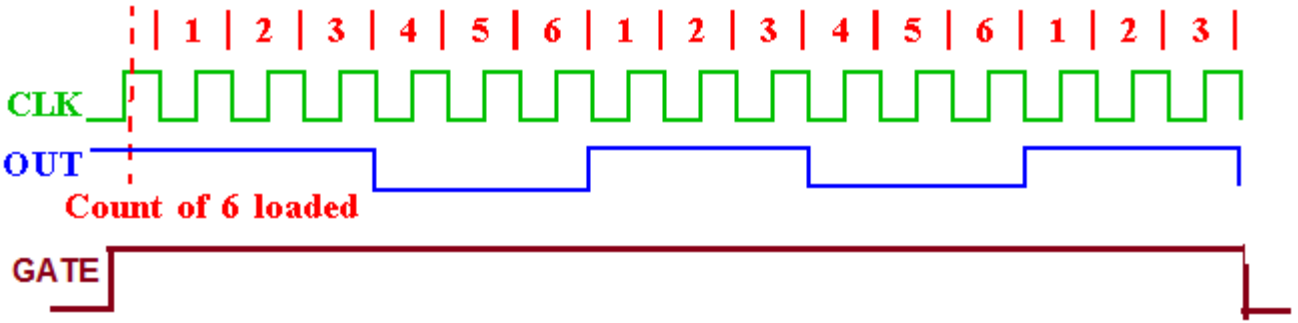


Modes of Operation

Square wave rate generator (mode 3)

(Initial value N= 6)

The counter decrements by 2 on each clock pulse & keep OUTPUT in one state. When the count becomes zero, the initial count is reloaded again , the counting starts again by decrementing 2 & the OUTPUT switches to opposite logic state. If initial count is odd, the Output is high for (N+1)/2 & low for (N-1)/2 CLK pulses.

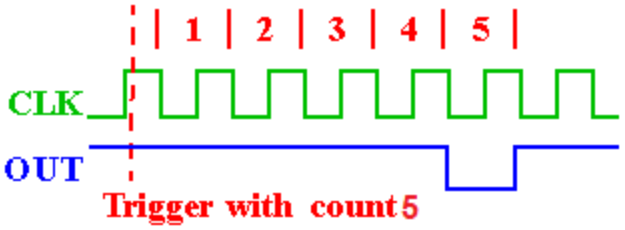


Modes of Operation

Soft ware triggered (strobed counter) mode 4

(Initial value N= 5)

After 4 pulses, the Output goes low for 1 clock period. When the counting starts, OUTPUT becomes high. No need to start the timer with GATE, the timer will start by software instruction.



Modes of Operation

Hard ware triggered (strobed counter) mode 5

Similar to mode 4, except the counting will be started by hardware GATE trigger. (gate = high pulse just to start counting).

Output of mode 2= mode 4 =mode 5

Difference

Mode 2→ gate high during counting

Mode 4→ no gate signal required

Mode 5→ high pulse at gate