**EXPERIMENT 09**

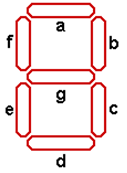
**BCD TO 7-SEGMENT CODE CONVERTER**

***Objective:***

***Equipment Required:***

***Seven Segment LED Display:***

Decimal digits from 0 to 9 can be shown using a 7–segment LED display unit. This unit shows one decimal digit using 7 LED segments to form the numbers from 0 to 9. These 7-segments are, a, b, c, d, e, f, g



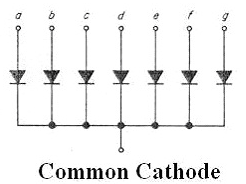
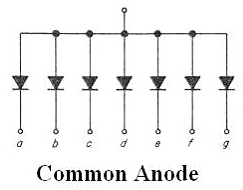
7-Segment Display

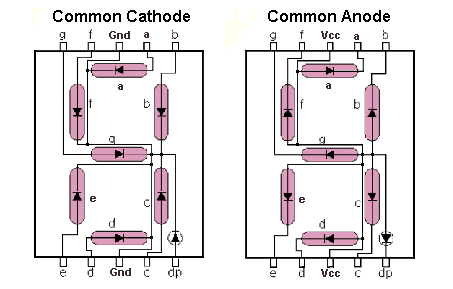
A BCD-to-seven-segment decoder (7448) is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig.(a) . The numeric display chosen to represent the decimal digit is shown in Fig.(b) .

**Two types of 7 Segment Displays**

*Segment Designation:*

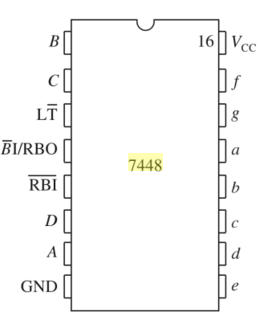
*Numerical Designation:*



***Different decoder IC with different display***

***Pin configuration***



7448-IC Pin Configuratio

***Procedure:***

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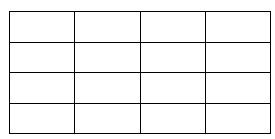
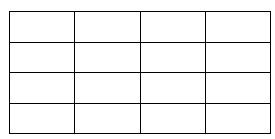
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***Design of BCD to seven segment code converter***

Using truth tables and Karnaugh maps, design the BCD-to-seven-segment decoder using minimum number of gates.

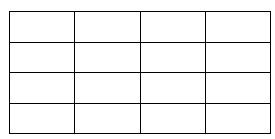
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| i3 | i2 | i1 | i0 | Decimal  Digit | Display | a | b | c | d | e | f | g |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |
| Rest of the combinations | | | | | | x | x | x | x | x | x | x |

***K-map***

** **

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***Observation and conclusions:***

***Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Instructor’s Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

**EXPERIMENT 10**

**IMPLEMENTATION OF LATCHES (NOR, NAND) AND DQ-FLIP FLOP**

***Objective:***

***Equipment Required:***

***Background Theory***

The elements used to store binary information in sequential circuits are called latches and flip-flops. A storage element can maintain a binary state as long as power is delivered to the circuit until directed by an input signal to switch states. The major differences among the various types of latches and flip-flops are the number of inputs they possess and the manner inputs affect the binary state. The most basic storage elements are latches, which uses feedback to lock onto and hold data, from which flip-flops are usually constructed. Although latches are most often used within flip-flops, they can also be used with more complex clocking methods to implement sequential circuits directly.

**NOR LATCHE**

***Truth table***

|  |  |  |
| --- | --- | --- |
| ***A*** | ***B*** | ***Y*** |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

***Logic Diagram***

**NOR LATCHE**

***Truth table***

|  |  |  |
| --- | --- | --- |
| ***A*** | ***B*** | ***Y*** |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

***Logic Diagram***

**Flip Flops**

A flip-flop is usually constructed by combining two same or different types of latches. Flip-flop circuits are constructed in such a way as to make them operate properly when they are a part of a sequential circuit that employs a single clock. Note that the problem with the latch is that as soon as an input changes, shortly thereafter the corresponding output changes to match it. This is what allows a change on a latch output to produce additional changes at other latch outputs while the clock pulse is at logic 1. The key to the proper operation of flip-flops is to prevent them from being transparent. In a flip-flop, before an output can change, the path from its inputs to its outputs is broken. So a flip-flop cannot “see” the change of its output or of the outputs of other, like flip-flops at its input during the same clock pulse. Thus, the new state of a flip-flop depends only on the immediately preceding state, and the flip-flops do not go through multiple changes of state. The edge triggered D flip flop avoids the problem of the RS invalid output states by not allowing the invalid states. The JK flip flop is a clocked RS flip flop with additional logic to replace the RS invalid output states with a new mode called toggle. Toggle causes the flip flop to change to the state opposite to its present state.

***D-Flip Flop***

***Truth table***

|  |  |  |
| --- | --- | --- |
| ***C*** | ***D*** | ***Q*** |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

***Logic Diagram***

***Procedure***

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

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***Observations and Conclusions:***

***Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Marks Obtained:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Instructor’s Signature:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

**EXPERIMENT 11**

**IMPLEMENTATION OF JK AND T-FLIP FLOP**

***Objectives:***

***Equipment Required:***

***Description:***

**Flip Flops**

A flip-flop is usually constructed by combining two same or different types of latches. Flip-flop circuits are constructed in such a way as to make them operate properly when they are a part of a sequential circuit that employs a single clock. Note that the problem with the latch is that as soon as an input changes, shortly thereafter the corresponding output changes to match it. This is what allows a change on a latch output to produce additional changes at other latch outputs while the clock pulse is at logic 1. The key to the proper operation of flip-flops is to prevent them from being transparent. In a flip-flop, before an output can change, the path from its inputs to its outputs is broken. So a flip-flop cannot “see” the change of its output or of the outputs of other, like flip-flops at its input during the same clock pulse. Thus, the new state of a flip-flop depends only on the immediately preceding state, and the flip-flops do not go through multiple changes of state. The edge triggered D flip flop avoids the problem of the RS invalid output states by not allowing the invalid states. The JK flip flop is a clocked RS flip flop with additional logic to replace the RS invalid output states with a new mode called toggle. Toggle causes the flip flop to change to the state opposite to its present state.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ***C*** | ***J*** | ***K*** | ***Q*** | ***Q+*** |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

**JK- FLIP FLOP**

***Truth table***

***Logic Diagram***

**T- FLIP FLOP**

***Truth table***

|  |  |  |  |
| --- | --- | --- | --- |
| ***C*** | ***T*** | ***Q*** | ***Q+*** |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

***Logic Diagram***

***Procedure***

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

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***Observations and Conclusions:***

***Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Marks Obtained:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Instructor’s Signature:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

**EXPERIMENT 12**

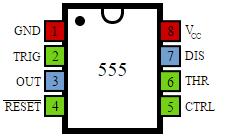
**Clock Generation Using 555 Timer**

***Objectives:***

***Equipment Required:***

***Introduction to 555 Timer IC***

The 8-pin 555 timer must be one of the most useful chips ever made and it is used in many projects. With just a few external components it can be used to build many circuits, not all of them involve timing.



**Figure 12.5 Pin Configurations of 555**

***Pin Description***

***Trigger input:*** when <1/3Vs ('active low') this makes the output high (+Vs). It monitors thedischarging of the timing capacitor in an astable circuit. It has a high input impedance > 2M

.

***Threshold input*:** when >2/3Vs ('active high') this makes the output low (0V)\*. It monitorsthe charging of the timing capacitor in astable and monostable circuits. It has a high input impedance > 10M .

\* providing the trigger input is > 1/3 Vs, otherwise the trigger input will override the threshold input and hold the output high (+Vs).

***Reset input:*** when less than about 0.7V ('active low') this makes the output low

(0V), overriding other inputs. When not required it should be connected to +Vs. It has an input impedance of about 10K.

***Control input:*** this can be used to adjust the threshold voltage which is set internally to be2/3 Vs. Usually this function is not required and the control input is connected to 0V with a

0.01μF capacitor to eliminate electrical noise. It can be left unconnected if noise is not a problem.

*The* ***discharge pin*** is not an input, but it is listed here for convenience. It is connected to 0V when the timer output is low and is used to discharge the timing capacitor in astable and monostable circuits.

***555 Astable***

An astable circuit produces a 'square wave', this is a digital waveform with sharp transitions between low (0V) and high (+Vs). Note that the durations of the low and high states may be different. The circuit is called an astable because it is not stable in any state: the output is continually changing between 'low' and 'high’. The time period (T) of the square wave is the time for one complete cycle, but it is usually better to consider frequency (f) which is the number of cycles per second

***Circuit Diagram:***

***Equation:***

***Procedure:***

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

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***Frequency Calculations of Generated Clock:***

|  |  |  |
| --- | --- | --- |
| ***C1*** | ***R2=***  ***R1=*** | ***R2=***  ***R1=*** |
|  |  |  |
|  |  |  |
|  |  |  |

***Observations and Conclusions:***

***Date: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Marks Obtained:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***

***Instructor’s Signature:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_***