Digital Logic & Design(Theory)

Program: BS(SE)

Course Codes: SEC-201

EDP Codes: 102002015

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Mid-Term Assignment

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Q.1 Convert each of the following:

a. $45.25_{10} = (\ ?\ )_{2}$

b. $10000000.1010_{2} = (\ ?\ )_{10}$

c. $4D7F_{16} = (\ ?\ )_{10}$

d. $128_{10} = (\ ?\ )_{16}$

e. $3A6F_{16} = (\ ?\ )_{2}$

f. $1100001111100101_{2} = (\ ?\ )_{16}$

g. $6173_{8} = (\ ?\ )_{10}$

h. $169_{10} = (\ ?\ )_{8}$

i. $2A7D_{16} = (\ ?\ )_{8}$

j. $11111111_{2} = \pm (\ ?\ )_{10}$ hint: [use 2's complement form]

k. $-12_{10} = (\ ?\ )_{2}$ hint: [use 2's complement form]

l. $198_{10} = (\ ?\ )_{BCD}$

m. $100001110000_{BCD} = (\ ?\ )_{10}$

n. $1001010_{2} = (\ ?\ )_{Gray}$

o. $10101111_{Gray} = (\ ?\ )_{2}$

p. $0100\ 0001 = (\ ?\ )_{ASCII}$

q. $111000 = (?111000)_{Even\ parity}$

Q.2 Calculate each of the following:

a. $01111111_2 - 00000111_2$ hint: [use 2's complement form]

b. $01101010_2 \times 11110001_2$ hint: [use 2's complement form]

c. $10001000_2 \div 00100010_2$ hint: [use 2's complement form]

d. $6D_{16} - 3F_{16}$ hint: [use 2's complement form]

e. $00010110_{BCD} + 0001\ 0101_{BCD} = (\ ?\ )_{10}$ hint: [take care of invalid BCD code]

Q.3 Apply CRC to the data bits 11010011_2 using the generator code 1010_2 to produce the transmitted CRC code.

Q.4 Assume that the code produced in problem Q.3 incurs an error in the most significant bit during transmission. Apply CRC to detect the error.

Q.5 The input waveforms in Figure 1 is applied to a 3-input AND gate. Show the output waveform in proper relation to the inputs with a timing diagram.

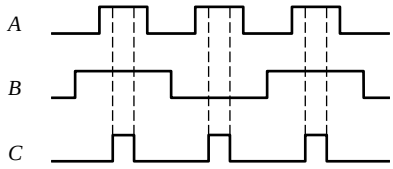

FIGURE 1

Q.6 Repeat Q.5 for a 3-input OR gate.

Q.7 Repeat Q.5 for a 3-input NAND gate.

Q.8 Repeat Q.5 for a 3-input NOR gate.

Q.9 The input waveforms in Figure 2 is applied to a XOR gate. Show the output waveform in proper relation to the inputs with a timing diagram.

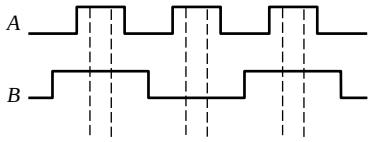

FIGURE 2

Q.10 Repeat Q.9 for XNOR gate.

Q.11 Using Boolean algebra techniques, simplify the following expressions as much as possible:

$$A\overline{B} + A\overline{B}C + A\overline{B}CD + A\overline{B}CDE$$

Q.12 Convert the following expressions to satndard SOP forms: $(C + D)(\overline{A} + D)$

Q.13 Write the standard POS expression using the standard SOP expression obtained in Q.12.

Q.14 Draw a single truth for both the standard POS and standard SOP expression obtained in Q.12 and Q.13.

Q.15 Use a Karnaugh map to simplify the following expression to a minimum SOP form:

$\bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$

Q.16 Obtain the minimum POS expression form the Karnaugh map used in Q.15.

Q.17 Write the output expression for circuit in Figure 3.

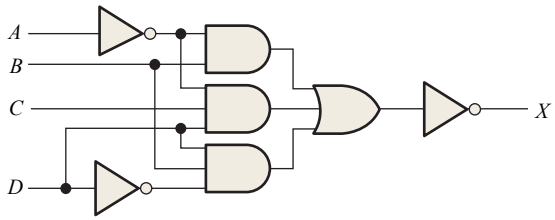

FIGURE 3

Q.18 Implement the logic circuits in Figure 3 using only NOR gates.

Q.19 Implement the logic circuits in Figure 3 using only NOR gates.

Q.20 Implement a logic circuit for the truth table in Table 1.

TABLE 1

Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Wish You All the Best