Program: BC (SE)

Subject: Digital Logic Design (Theory)

Assignment Number: 03

Course Code: SEC-201

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Spring Semester 2020

Q.1 Using Boolean notation, write an expression that is a 0 only when all of its variables (A, B, C, and D) are 0s.

Q.2 Write an expression that is a 1 when one or more of its variables (A, B, C, D, and E) are 0s.

Q.3 Write an expression that is a 0 when one or more of its variables (A, B, and C) are 0s.

Q.4 Evaluate the following operations:

(a) $0 + 0 + 0 + 1$ **(b)** $1 \cdot 0 \cdot 1 \cdot 0$ **(c)** $1 \cdot 0 + 1 \cdot 0 + 0 \cdot 1 + 0 \cdot 1$

Q.5 Find the values of the variables that make each product term 1 and each sum term 0.

(a) $\overline{A}\,\overline{B}C$ **(b)** $\overline{A} + \overline{B} + C$

Q.6 Apply DeMorgan's theorems to the following:

(a) $\overline{\overline{(ABC)(\overline{EFG})} + \overline{(\overline{HIJ})(\overline{KLM})}}$ **(b)** $\overline{\overline{(\overline{A} + B)(\overline{C} + D)(\overline{E} + F)(\overline{G} + H)}}$

Q.7 Write the Boolean expression for each of the logic circuits in Figure 01.

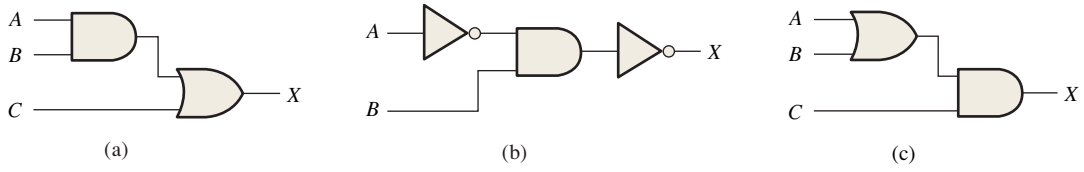

FIGURE 01

Q.8 Draw the logic circuit represented by the following expression: $AB + \overline{AB}$

Q.9 **(a)** Draw a logic circuit for the case where the output, ENABLE, is HIGH only if the inputs, ASSERT and READY, are both LOW.

(b) Draw a logic circuit for the case where the output, HOLD, is HIGH only if the input, LOAD, is LOW and the input, READY, is HIGH.

Q.10 Develop the truth table for each of the circuits in Figure 02.

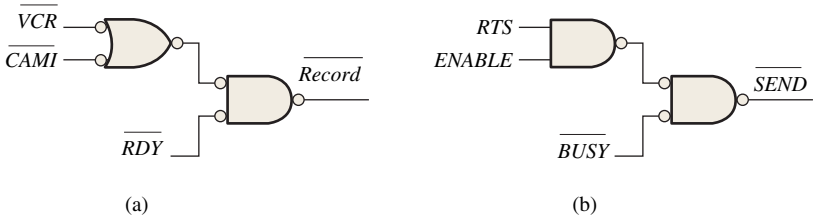

FIGURE 02

Q.11 Construct a truth table for each of the following Boolean expressions:

(a) $(A + B)(B + C)(C + A)$ **(b)** $\overline{A}B + \overline{B}C + \overline{C}A$

Q.12 Using Boolean algebra techniques, simplify the following expressions as much as possible:

(a) $A(A + B)$ **(b)** $A(A + \overline{A}B)$ **(c)** $BC + \overline{B}C$

(d) $A(A + \overline{A}B)$ **(e)** $A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}C$ **(f)** $BC + (\overline{B} + C)D + BC$

(g) $BCD[BC + \overline{D}(CD + BD)]$ **(h)** $A\overline{B} + A\overline{B}C + A\overline{B}CD + A\overline{B}CDE$

Q.13 Determine which of the logic circuits in Figure 03 are equivalent.

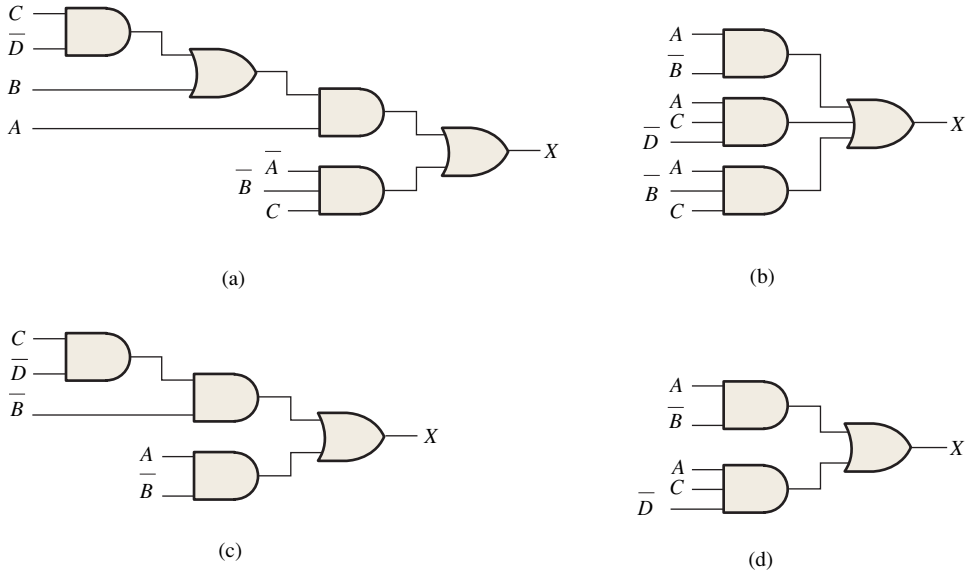

FIGURE 03

Q.14 Convert the following expressions to sum-of-product (SOP) forms:

(a) $(C + D)(A + \overline{D})$ **(b)** $(A + C)(CD + AC)$ **(c)** $B + C[BD + (C + \overline{D})E]$

(d) $A(A\overline{D} + C)$ **(e)** $BC + DE(B\overline{C} + DE)$ **(f)** $BC(\overline{C}\,\overline{D} + CE)$

Q.15 Convert each SOP expression obtained in Q.14 to standard SOP form.

Q.16 Convert each standard SOP expression obtained in Q.15 to standard POS form.

Q.17 Develop a truth table for each standard SOP expression obtained in Q.15.

Q.18 Develop a truth table for each standard POS expression obtained in Q.16.

Q.19 Derive a standard SOP and a standard POS expression form truth table in Table 01.

Q.20 Use a Karnaugh map to find the minimum SOP form for each expression:

(a) $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\overline{B}C + A\overline{B}C$ **(b)** $AC(\overline{B} + C)$

(c) $\overline{A}(BC + B\overline{C}) + A(BC + B\overline{C})$ **(d)** $\overline{A}\,\overline{B}\,\overline{C} + A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + AB\overline{C}$

(e) $A + B\overline{C} + CD$ **(f)** $\overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + ABCD + ABC\overline{D}$

(g) $\overline{A}\,\overline{B} + A\overline{B} + \overline{C}\,\overline{D} + C\overline{D}$ **(h)** $\overline{A}B(\overline{C}\,\overline{D} + \overline{C}D) + AB(\overline{C}\,\overline{D} + \overline{C}D) + A\overline{B}\,\overline{C}D$

Q.21 Reduce the function specified in truth Table 02 to its minimum SOP form by using a Karnaugh map.

Q.22 Use the Karnaugh map method to implement the minimum SOP expression for the logic function specified in truth Table 03.

Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table 01

Inputs			Output
A	*B*	*C*	*X*
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 02

Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Table 03

Q.23 Use a Karnaugh map to find the minimum POS for each expression:

(a) $(A + B + C)(\overline{A} + \overline{B} + \overline{C})(A + \overline{B} + C)$

(b) $(X + \overline{Y})(\overline{X} + Z)(X + \overline{Y} + \overline{Z})(\overline{X} + \overline{Y} + Z)$

(c) $A(B + \overline{C})(\overline{A} + C)(A + \overline{B} + C)(\overline{A} + B + \overline{C})$

Q.24 For the function specified in Table 02, determine the minimum POS expression using a Karnaugh map.

Q.25 Determine the minimum POS expression for the function in Table 03.

Q.26 Convert each of the following POS expressions to minimum SOP expressions using a Karnaugh map:

(a) $(A + \overline{B})(A + \overline{C})(\overline{A} + \overline{B} + C)$

(b) $(\overline{A} + B)(\overline{A} + \overline{B} + \overline{C})(B + \overline{C} + D)(A + \overline{B} + C + \overline{D})$