Department of Electrical Engineering
Assignment 3
Date:25/06/2020

Course Details

Course Title: _____ **Module:** _____
Instructor: _____ **Total Marks:** _____

Student Details

Name: _____ **Student ID:** _____

Q 1.		Design an area efficient layout diagram for the CMOS logic shown below F= AB+(CD)E
Q 2.		Give the subsystem design considerations of a four-bit adder.
Q 3.		Discuss the VLSI design issues and design trends. Explain with neat diagram, simple parity check code.
Q 4		Does the inverter with a lower VOL always have the shorter high-to-low switching time? Justify your answer.
Q 5.		Design 8×1 MUX using two 4:1 MUX and one 2:1 MUX along with its diagram. Implement 8×1 multiplexer in VHDL using structural modelling style. **GOOD LUCK**