The point is this: You don't have to use Eq. (8-11) to calculate emitter current when the voltage divider is stiff. Even when the voltage divider is firm, the use of Eq. (8-11) will improve the calculation for emitter current only by at most 10 percent. Unless otherwise indicated, from now on all analysis of VDB circuits will use the simplified method.

8-3 VDB Load Line and Q Point

Because of the stiff voltage divider in Fig. 8-6, the emitter voltage is held constant at 1.1 V in the following discussion.

The Q Point

The Q point was calculated in Sec. 8-1. It has a collector current of 1.1 mA and a collector-emitter voltage of 4.94 V. These values are plotted to get the Q point shown in Fig. 8-6. Since voltage-divider bias is derived from emitter bias, the Q point is virtually immune to changes in current gain. One way to move the Q point in Fig. 8-6 is by varying the emitter resistor.

For instance, if the emitter resistance is changed to 2.2 kΩ, the collector current decreases to:

$$I_E = \frac{1.1\text{ V}}{2.2\text{ k}\Omega} = 0.5\text{ mA}$$

The voltages change as follows:

$$V_C = 10\text{ V} - (0.5\text{ mA})(3.6\text{ k}\Omega) = 8.2\text{ V}$$

and

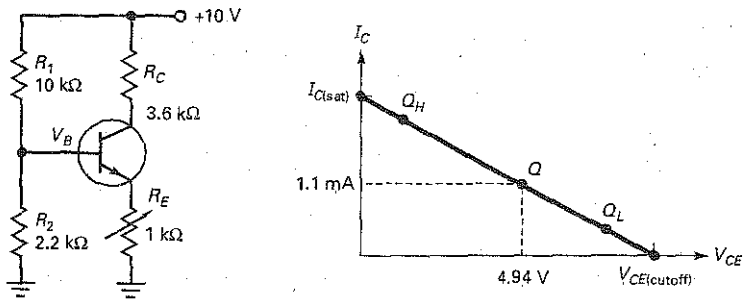
$$V_{CE} = 8.2\text{ V} - 1.1\text{ V} = 7.1\text{ V}$$

Therefore, the new Q point will be Q_L and will have coordinates of 0.5 mA and 7.1 V.

On the other hand, if we decrease the emitter resistance to 510 Ω, the emitter current increases to:

$$I_E = \frac{1.1\text{ V}}{510\,\Omega} = 2.15\text{ mA}$$

Figure 8-6 Calculating the Q point.



and the voltages change to:

$$V_C = 10\text{ V} - (2.15\text{ mA})(3.6\text{ k}\Omega) = 2.26\text{ V}$$

and

$$V_{CE} = 2.26\text{ V} - 1.1\text{ V} = 1.16\text{ V}$$

In this case, the Q point shifts to a new position at Q_H with coordinates of 2.15 mA and 1.16 V.

Q Point in Middle of Load Line

V_{CC}, R_1, R_2, and R_C control the saturation current and the cutoff voltage. A change in any of these quantities will change $I_{C(\text{sat})}$ and/or $V_{CE(\text{cutoff})}$. Once the designer has established the values of the foregoing variables, the *emitter resistance* is varied to set the Q point at any position along the load line. If R_E is too large, the Q point moves into the cutoff point. If R_E is too small, the Q point moves into saturation. Some designers set the Q point at the middle of the load line.

GOOD TO KNOW

Centering the Q point on a transistor load line is important because it allows for the maximum ac output voltage from the amplifier. Centering the Q point on the dc load line is sometimes referred to as *midpoint bias*.

VDB Design Guideline

Fig. 8-7 shows a VDB circuit. This circuit will be used to demonstrate a simplified design guideline to establish a stable Q point. This design technique is suitable for most circuits, but it is only a guideline. Other design techniques can be used.

Before starting the design, it is important to determine the circuit requirements or specifications. The circuit is normally biased for V_{CE} to be at a midpoint value with a specified collector current. You also need to know the value of V_{CC} and the range of β_{dc} for the transistor being used. Also, be sure the circuit will not cause the transistor to exceed its power dissipation limits.

Start by making the emitter voltage approximately one-tenth of the supply voltage:

$$V_E = 0.1\ V_{CC}$$

Next, calculate the value of R_E to set up the specified collector current:

$$R_E = \frac{V_E}{I_E}$$

Since the Q point needs to be at approximately the middle of the dc load line, about 0.5 V_{CC} appears across the collector-emitter terminals. The remaining 0.4 V_{CC} appears across the collector resistor; therefore:

$$R_C = 4\ R_E$$

Next, design for a stiff voltage divider using the 100:1 rule:

$$R_{TH} \leq 0.01\ \beta_{dc}\ R_E$$

Usually, R_2 is smaller than R_1. Therefore, the stiff voltage divider equation can be simplified to:

$$R_2 \leq 0.01\ \beta_{dc}\ R_E$$

You may also choose to design for a firm voltage divider by using the 10:1 rule:

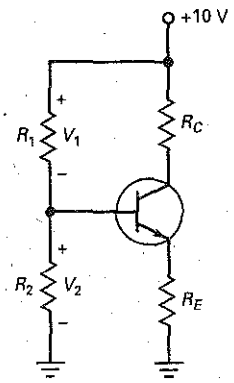
$$R_2 \leq 0.1\ \beta_{dc}\ R_E$$

In either case, use the minimum-rated β_{dc} value at the specified collector current.

Finally, calculate R_1 by using proportion:

$$R_1 = \frac{V_1}{V_2}\ R_2$$

Figure 8-7 VDB design.



Example 8–4

For the circuit shown in Fig. 8-7, design the resistor values to meet these specifications:

$V_{CC} = 10$ V V_{CE} @ midpoint

$I_C = 10$ mA 2N3904's $\beta_{dc} = 100$–300

SOLUTION First, establish the emitter voltage by:

$$V_E = 0.1\ V_{CC}$$

$$V_E = (0.1)\ (10\ \text{V}) = 1\ \text{V}$$

The emitter resistor is found by:

$$R_E = \frac{V_E}{I_E}$$

$$R_E = \frac{1\ \text{V}}{10\ \text{mA}} = 100\ \Omega$$

The collector resistor is:

$$R_C = 4\ R_E$$

$$R_C = (4)\ (100\ \Omega) = 400\ \Omega \text{ (use } 390\ \Omega)$$

Next, choose either a stiff or firm voltage divider. A stiff value of R_2 is found by:

$$R_2 \leq 0.01\ \beta_{dc}\ R_E$$

$$R_2 \leq (0.01)\ (100)\ (100\ \Omega) = 100\ \Omega$$

Now, the value of R_1 is:

$$R_1 = \frac{V_1}{V_2} R_2$$

$$V_2 = V_E + 0.7\ \text{V} = 1\ \text{V} + 0.7\ \text{V} = 1.7\ \text{V}$$

$$V_1 = V_{CC} - V_2 = 10\ \text{V} - 1.7\ \text{V} = 8.3\ \text{V}$$

$$R_1 = \left(\frac{8.3\ \text{V}}{1.7\ \text{V}}\right)(100\ \Omega) = 488\ \Omega \text{ (use } 490\ \Omega)$$

PRACTICE PROBLEM 8–4 Using the given VDB design guidelines, design the VDB circuit of Fig. 8-7 to meet these specifications:

$V_{CC} = 10$ V V_{CE} @ midpoint stiff voltage divider

$I_C = 1$ mA $\beta_{dc} = 70$-200

8–4 Two-Supply Emitter Bias

Some electronic equipment has a power supply that produces both positive and negative supply voltages. For instance, Fig. 8-8 shows a transistor circuit with two power supplies: +10 and −2 V. The negative supply forward biases the emitter