Example 7-6

Suppose the base resistance of Fig. 7-7*a* is increased to 1 MΩ. Is the transistor still saturated?

SOLUTION Assume the transistor is operating in the active region, and see whether a contradiction arises. Ideally, the base current is 10 V divided by 1 MΩ, or 10 μA. The collector current is 50 times 10 μA, or 0.5 mA. This current produces 5 V across the collector resistor. Subtract 5 from 20 V to get:

$$V_{CE} = 15 \text{ V}$$

There is no contradiction here. If the transistor were saturated, we would have calculated a negative number or, at most, 0 V. Because we got 15 V, we know that the transistor is operating in the active region.

Example 7-7

Suppose the collector resistance of Fig. 7-7*a* is decreased to 5 kΩ. Does the transistor remain in the saturation region?

SOLUTION Assume the transistor is operating in the active region, and see whether a contradiction arises. We can use the same approach as in Example 7-6, but for variety, let us try the second method.

Start by calculating the saturation value of the collector current. Visualize a short between the collector and the emitter. Then you can see that 20 V will be across 5 kΩ. This gives a saturated collector current of:

$$I_{C(\text{sat})} = 4 \text{ mA}$$

The base current is ideally 10 V divided by 100 kΩ, or 0.1 mA. The collector current is 50 times 0.1 mA, or 5 mA.

There is a contradiction. The collector current cannot be greater than 4 mA because the transistor saturates when $I_C = 4$ mA. The only thing that can change at this point is the current gain. The base current is still 0.1 mA, but the current gain decreases to:

$$\beta_{\text{dc(sat)}} = \frac{4 \text{ mA}}{0.1 \text{ mA}} = 40$$

This reinforces the idea discussed earlier. A transistor has two current gains, one in the active region and another in the saturation region. The second is equal to or smaller than the first.

PRACTICE PROBLEM 7-7 If the collector resistance of Fig. 7-7*a* is 4.7 kΩ, what value of base resistor would produce hard saturation using the 10:1 design rule?

7-5 The Transistor Switch

Base bias is useful in *digital circuits* because these circuits are usually designed to operate at saturation and cutoff. Because of this, they have either low output voltage or high output voltage. In other words, none of the *Q* points between saturation and cutoff are used. For this reason, variations in the Q point don't matter, because the transistor remains in saturation or cutoff when the current gain changes.

Here is an example of using a base-biased circuit to switch between saturation and cutoff. Figure 7-8*a* shows an example of a transistor in hard saturation. Therefore, the output voltage is approximately 0 V. This means the Q point is at the upper end of the load line (Fig. 7-8*b*).

When the switch opens, the base current drops to zero. Because of this, the collector current drops to zero. With no current through the 1 kΩ, all the collector supply voltage will appear across the collector-emitter terminals. Therefore, the output voltage rises to +10 V. Now, the Q point is at the lower end of load line (see Fig. 7-8*b*).

The circuit can have only two output voltages: 0 or +10 V. This is how you can recognize a digital circuit. It has only two output levels: low or high. The exact values of the two output voltages are not important. All that matters is that you can distinguish the voltages as low or high.

Digital circuits are often called *switching circuits* because their Q point switches between two points on the load line. In most designs, the two points are saturation and cutoff. Another name often used is **two-state circuits,** referring to the low and high outputs.

Example 7-8

The collector supply voltage of Fig. 7-8*a* is decreased to 5 V. What are the two values of the output voltage? If the saturation voltage $V_{CE(\text{sat})}$ is 0.15 V and the collector leakage current I_{CEO} is 50 nA, what are the two values of the output voltage?

SOLUTION The transistor switches between saturation and cutoff. Ideally, the two values of output voltage are 0 and 5 V. The first voltage is the voltage across the saturated transistor, and the second voltage is the voltage across the cutoff transistor.

If you include the effects of saturation voltage and collector leakage current, the output voltages are 0.15 and 5 V. The first voltage is the voltage across the saturated transistor, which is given as 0.15 V. The second voltage is the collector-emitter voltage with 50 nA flowing through 1 kΩ:

$$V_{CE} = 5\text{ V} - (50\text{ nA})(1\text{ k}\Omega) = 4.99995\text{ V}$$

which rounds to 5 V.

Unless you are a designer, it is a waste of time to include the saturation voltage and the leakage current in your calculations of switching circuits. With switching circuits, all you need is two distinct voltages: one low and the other high. It doesn't matter whether the low voltage is 0, 0.1, 0.15 V, and so on. Likewise, it doesn't matter whether the high voltage is 5, 4.9, or 4.5 V. All that usually matters in the analysis of switching circuits is that you can distinguish the low voltage from the high voltage.

PRACTICE PROBLEM 7-8 If the circuit of Fig. 7-8*a* used 12 V for its collector and base supply voltage, what are the two values of switched output voltage? ($V_{CE(\text{sat})} = 0.15$ V and $I_{CEO} = 50$ nA)