GOOD TO KNOW

There is often a lot of confusion in textbooks and in manufacturers' data sheets regarding the terms *cutoff* and *pinchoff*. $V_{GS(off)}$ is the value of V_{GS} that completely pinches off the channel, thus reducing the drain current to zero. On the other hand, the pinchoff voltage is the value of V_{DS} at which I_D levels off with $V_{GS} = 0$ V.

The bottom curve is important. Notice that a V_{GS} of -4 V reduces the drain current to almost zero. This voltage is called the **gate-source cutoff voltage** and is symbolized by $V_{GS(off)}$ on data sheets. At this cutoff voltage the depletion layers touch. In effect, the conducting channel disappears. This is why the drain current is approximately zero.

In Fig. 13-5, notice that

$$V_{GS(off)} = -4 \text{ V} \qquad \text{and} \qquad V_P = 4 \text{ V}$$

This is not a coincidence. The two voltages always have the same magnitude because they are the values where the depletion layers touch or almost touch. Data sheets may list either quantity, and you are expected to know that the other has the same magnitude. As an equation:

$$V_{GS(off)} = -V_P \tag{13-2}$$

Example 13-2

An MPF4857 has $V_P = 6$ V and $I_{DSS} = 100$ mA. What is the ohmic resistance? The gate-source cutoff voltage?

SOLUTION The ohmic resistance is:

$$R_{DS} = \frac{6 \text{ V}}{100 \text{ mA}} = 60 \ \Omega$$

Since the pinchoff voltage is 6 V, the gate-source cutoff voltage is:

$$V_{GS(off)} = -6 \text{ V}$$

PRACTICE PROBLEM 13-2 A 2N5484 has a $V_{GS(off)} = -3.0$ V and $I_{DSS} = 5$ mA. Find its ohmic resistance and V_p values.

13-3 The Transconductance Curve

GOOD TO KNOW

The transconductance curve of a JFET is unaffected by the circuit or configuration in which the JFET is used.

The **transconductance curve** of a JFET is a graph of I_D versus V_{GS}. By reading the values of I_D and V_{GS} of each drain curve in Fig. 13-5, we can plot the curve of Fig. 13-6*a*. Notice that the curve is nonlinear because the current increases faster when V_{GS} approaches zero.

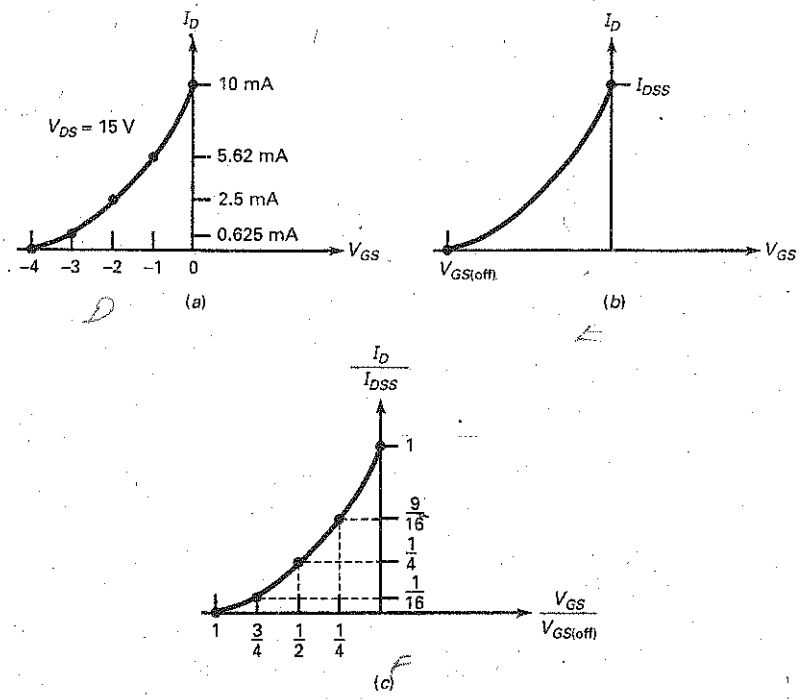
Any JFET has a transconductance curve like Fig. 13-6*b*. The end points on the curve are $V_{GS(off)}$ and I_{DSS}. The equation for this graph is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \tag{13-3}$$

Because of the squared quantity in this equation, JFETs are often called *square-law devices*. The squaring of the quantity produces the nonlinear curve of Fig. 13-6*b*.

Figure 13-6*c* shows a *normalized transconductance curve*. *Normalized* means that we are graphing ratios like I_D/I_{DSS} and $V_{GS}/V_{GS(off)}$.

Figure 13-6 Transconductance curve.



In Fig. 13-6*c*, the half-cutoff point

$$\frac{V_{GS}}{V_{GS(off)}} = \frac{1}{2}$$

produces a normalized current of:

$$\frac{I_D}{I_{DSS}} = \frac{1}{4}$$

In words: When the gate voltage is half the cutoff voltage, the drain current is one quarter of maximum.

Example 13-3

A 2N5668 has $V_{GS(off)} = -4$ V and $I_{DSS} = 5$ mA. What are the gate voltage and drain current at the half cutoff point?

SOLUTION At the half cutoff point:

$$V_{GS} = \frac{-4 \text{ V}}{2} = -2 \text{ V}$$

and the drain current is:

$$I_D = \frac{5 \text{ mA}}{4} = 1.25 \text{ mA}$$

Example 13-4

A 2N5459 has $V_{GS(off)} = -8$ V and $I_{DSS} = 16$ mA. What is the drain current at the half cutoff point?

SOLUTION The drain current is one quarter of the maximum, or:

$$I_D = 4 \text{ mA}$$

The gate-source voltage that produces this current is -4 V, half of the cutoff voltage.

PRACTICE PROBLEM 13-4 Repeat Example 13-4 using a JFET with $V_{GS(off)} = -6$ V and $I_{DSS} = 12$ mA.

13-4 Biasing in the Ohmic Region

The JFET can be biased in the ohmic or in the active region. When biased in the ohmic region, the JFET is equivalent to a resistance. When biased in the active region, the JFET is equivalent to a current source. In this section, we discuss gate bias, the method used to bias a JFET in the ohmic region.

Gate Bias

Figure 13-7*a* shows **gate bias.** A negative gate voltage of $-V_{GG}$ is applied to the gate through biasing resistor R_G. This sets up a drain current that is less than I_{DSS}. When the drain current flows through R_D, it sets up a drain voltage of:

$$V_D = V_{DD} - I_D R_D \tag{13-4}$$

Gate bias is the worst way to bias a JFET in the active region because the Q point is too unstable.

For example, a 2N5459 has the following spreads between minimum and maximum: I_{DSS} varies from 4 to 16 mA, and $V_{GS(off)}$ varies from -2 to -8 V. Figure 13-7*b* shows the minimum and maximum transconductance curves. If a gate bias of -1 V is used with this JFET, we get the minimum and maximum Q points shown. Q_1 has a drain current of 12.3 mA, and Q_2 has a drain current of only 1 mA.

Hard Saturation

Although not suitable for active-region biasing, gate bias is perfect for ohmic-region biasing because stability of the Q point does not matter. Figure 13-7*c* shows how to bias a JFET in the ohmic region. The upper end of the dc load line has a drain saturation current of:

$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

To ensure that a JFET is biased in the ohmic region, all we need to do is use $V_{GS} = 0$ and:

$$I_{D(sat)} \ll I_{DSS} \tag{13-5}$$