Example 7–5

MultiSim

Suppose the base resistance of Fig. 7-6*a* is increased to 1 MΩ. What happens to the collector-emitter voltage if β_{dc} is 100?

SOLUTION Ideally, the base current would decrease to 15 μA, the collector current would decrease to 1.5 mA, and the collector-emitter voltage would increase to:

$$V_{CE} = 15 - (1.5 \text{ mA})(3 \text{ k}\Omega) = 10.5 \text{ V}$$

To a second approximation, the base current would decrease to 14.3 μA, and the collector current would decrease to 1.43 mA. The collector-emitter voltage would increase to:

$$V_{CE} = 15 - (1.43 \text{ mA})(3 \text{ k}\Omega) = 10.7 \text{ V}$$

PRACTICE PROBLEM 7–5 If the β_{dc} value of Example 7-5 changed to 150 due to a temperature change, find the new value of V_{CE}.

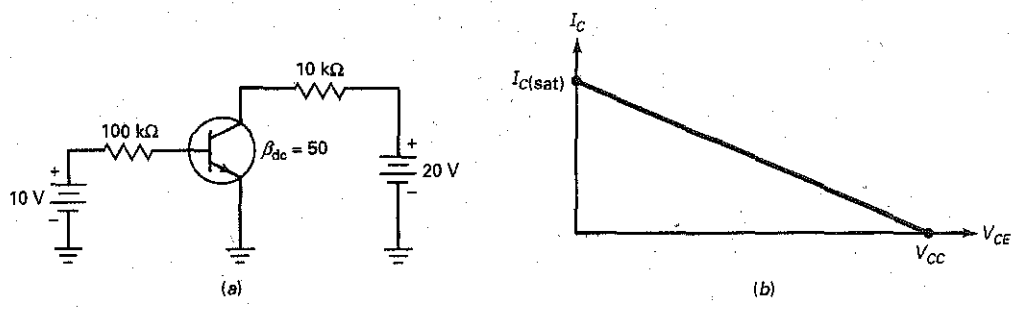
7–4 Recognizing Saturation

There are two basic kinds of transistor circuits: **amplifying** and **switching.** With amplifying circuits, the *Q* point must remain in the active region under all operating conditions. If it does not, the output signal will be distorted on the peak where saturation or cutoff occurs. With switching circuits, the *Q* point usually switches between saturation and cutoff. How switching circuits work, what they do, and why they are used will be discussed later.

Impossible Answers

Assume that the transistor of Fig. 7-7*a* has a breakdown voltage greater than 20 V. Then, we know that it is not operating in the breakdown region. Furthermore, we can tell at a glance that the transistor is not operating in the cutoff region because of the biasing voltages. What is not immediately clear, however, is whether the transistor is operating in the active region or the saturation region. It must be operating in one of these regions. But which?

Figure 7–7 (*a*) Base-biased circuit; (*b*) load line.



Troubleshooters and designers often use the following method to determine whether a transistor is operating in the active region or the saturation region. Here are the steps in using the method:

1. Assume that the transistor is operating in the active region.
2. Carry out the calculations for currents and voltages.
3. If an impossible result occurs in any calculation, the assumption is false.

An impossible answer means that the transistor is saturated. Otherwise, the transistor is operating in the active region.

Saturation-Current Method

For instance, Fig. 7-7*a* shows a base-biased circuit. Start by calculating the saturation current:

$$I_{C(sat)} = \frac{20\text{ V}}{10\text{ k}\Omega} = 2\text{ mA}$$

The base current is ideally 0.1 mA. Assuming a current gain of 50 as shown, the collector current is:

$$I_C = 50(0.1\text{ mA}) = 5\text{ mA}$$

The answer is impossible because the collector current cannot be greater than the saturation current. Therefore, the transistor cannot be operating in the active region; it must be operating in the saturation region.

Collector-Voltage Method

Suppose you want to calculate V_{CE} in Fig. 7-7*a*. Then you can proceed like this: The base current is ideally 0.1 mA. Assuming a current gain of 50 as shown, the collector current is:

$$I_C = 50(0.1\text{ mA}) = 5\text{ mA}$$

and the collector-emitter voltage is:

$$V_{CE} = 20\text{ V} - (5\text{ mA})(10\text{ k}\Omega) = -30\text{ V}$$

This result is impossible because the collector-emitter voltage cannot be negative. So the transistor cannot be operating in the active region; it must be operating in the saturation region.

Current Gain Is Less in Saturation Region

When you are given the current gain, it is usually for the active region. For instance, the current gain of Fig. 7-7*a* is shown as 50. This means that the collector current will be 50 times the base current, provided the transistor is operating in the active region.

When a transistor is saturated, the current gain is less than the current gain in the active region. You can calculate the saturated current gain as follows:

$$\beta_{dc(sat)} = \frac{I_{C(sat)}}{I_B}$$

In Fig. 7-7*a*, the saturated current gain is

$$\beta_{dc(sat)} = \frac{2\text{ mA}}{0.1\text{ mA}} = 20$$

Hard Saturation

A designer who wants a transistor to operate in the saturation region under all conditions often selects a base resistance that produces a current gain of 10. This is called **hard saturation,** because there is more than enough base current to saturate the transistor. For example, a base resistance of 50 kΩ in Fig. 7-7*a* will produce a current gain of:

$$\beta_{dc} = \frac{2\text{ mA}}{0.2\text{ mA}} = 10$$

For the transistor of Fig. 7-7*a*, it takes only

$$I_B = \frac{2\text{ mA}}{50} = 0.04\text{ mA}$$

to saturate the transistor. Therefore, a base current of 0.2 mA will drive the transistor deep into saturation.

Why does a designer use hard saturation? Recall that the current gain changes with collector current, temperature variation, and transistor replacement. To make sure that the transistor does not slip out of saturation at low collector currents, low temperatures, and so on, the designer uses hard saturation to ensure transistor saturation under all operating conditions.

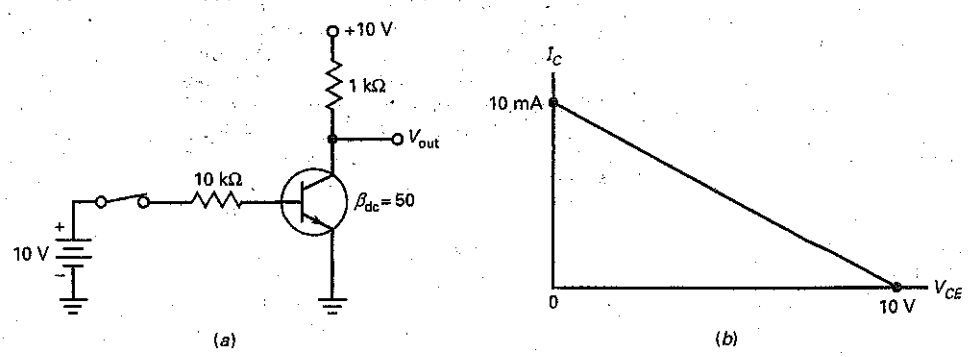
From now on, *hard saturation* will refer to any design that makes the saturated current gain approximately 10. **Soft saturation** will refer to any design in which the transistor is barely saturated, that is, in which the saturated current gain is only a little less than the active current gain.

Recognizing Hard Saturation at a Glance

Here is how you can quickly tell whether a transistor is in hard saturation. Often, the base supply voltage and the collector supply voltage are equal: $V_{BB} = V_{CC}$. When this is the case, a designer will use the 10 : 1 rule, which says to make the base resistance approximately 10 times as large as the collector resistance.

Figure 7-8*a* was designed by using the 10 : 1 rule. Therefore, whenever you see a circuit with a 10 : 1 ratio (R_B to R_C), you can expect it to be saturated.

Figure 7–8 (*a*) Hard saturation; (*b*) load line.



Example 7-6

Suppose the base resistance of Fig. 7-7*a* is increased to 1 MΩ. Is the transistor still saturated?

SOLUTION Assume the transistor is operating in the active region, and see whether a contradiction arises. Ideally, the base current is 10 V divided by 1 MΩ, or 10 μA. The collector current is 50 times 10 μA, or 0.5 mA. This current produces 5 V across the collector resistor. Subtract 5 from 20 V to get:

$$V_{CE} = 15 \text{ V}$$

There is no contradiction here. If the transistor were saturated, we would have calculated a negative number or, at most, 0 V. Because we got 15 V, we know that the transistor is operating in the active region.

Example 7-7

Suppose the collector resistance of Fig. 7-7*a* is decreased to 5 kΩ. Does the transistor remain in the saturation region?

SOLUTION Assume the transistor is operating in the active region, and see whether a contradiction arises. We can use the same approach as in Example 7-6, but for variety, let us try the second method.

Start by calculating the saturation value of the collector current. Visualize a short between the collector and the emitter. Then you can see that 20 V will be across 5 kΩ. This gives a saturated collector current of:

$$I_{C(sat)} = 4 \text{ mA}$$

The base current is ideally 10 V divided by 100 kΩ, or 0.1 mA. The collector current is 50 times 0.1 mA, or 5 mA.

There is a contradiction. The collector current cannot be greater than 4 mA because the transistor saturates when $I_C = 4$ mA. The only thing that can change at this point is the current gain. The base current is still 0.1 mA, but the current gain decreases to:

$$\beta_{dc(sat)} = \frac{4 \text{ mA}}{0.1 \text{ mA}} = 40$$

This reinforces the idea discussed earlier. A transistor has two current gains, one in the active region and another in the saturation region. The second is equal to or smaller than the first.

PRACTICE PROBLEM 7-7 If the collector resistance of Fig. 7-7*a* is 4.7 kΩ, what value of base resistor would produce hard saturation using the 10:1 design rule?

7-5 The Transistor Switch

Base bias is useful in *digital circuits* because these circuits are usually designed to operate at saturation and cutoff. Because of this, they have either low output voltage or high output voltage. In other words, none of the *Q* points between saturation