**Online Lab Plan Report**

**Instructor:Rashid Aleem**

**Lab:Electronic Circuit Design**

**Week 7**

**Experiment :-** Practical analysis of Peak detector using multisim software

**Software used:-**Multisim 11.0

**Procedure:-**A peak detector is a circuit outputting a dc voltage equal to the peak value of the applied AC voltage signal.In the positive half cycle ,diode is forward biased and capacitor starts charging.When input reaches its peak value capacitor gets charged to positive peak value.In negative half cycle,as input decreases ,diode is reversed biased and capacitor is isolated and holds the peak value of previous cycle called peak detector.741 op-amp will be used and output will be observed in oscilloscope.

**Steps:-**

(1)Right click on the breadboard and select place components. Then select all groups.

(2)Select Op-amp and in Op-amp section select 741.

(3)Click on place components and then select sources and in sources section select ground.

(4)The positive pin of the operational amplifier should be connected to AC source.

(5)The negative pin of the operational amplifier should be connected to diode .

(7)Connect the oscilloscope with the circuit and check the desired output.

After performing this experiment on multisim software students will be able to understand the basic concept of Peak detector..

**LAB NO: 12**

**“Practical analysis of peak detector”**

**Objective:**

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**Apparatus:**

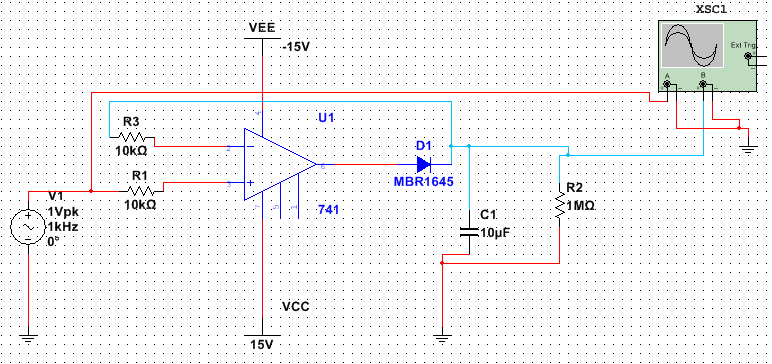
1. OP-Amp UA 741CP
2. Resistors
3. DC Power supplies
4. Function generator
5. Oscilloscope
6. Breadboard
7. Diode
8. Capacitor

**Theory:**

A peak detector is a circuit outputting a dc voltage equal to the peak value of the applied AC signal. In the positive half cycle, diode D is forward biased and capacitor C starts charging. When input reaches its peak value capacitor gets charged to positive peak value. In negative half cycle, as input decreases, diode D is reversed biased and capacitor is isolated and holds the peak value of previous cycle hence called as peak detector.

But in practice, output is taken across some load R**L**, so when input voltage decreases capacitor discharges through load R**L**. To avoid this select R**L** of very large value so that capacitor discharges very slowly hence almost holds the charge. Whatever charge it lost through RL is gets back in next half cycle.

**Circuit Diagram:**



**Procedure:**

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