Program: BC (CS)

Subject: Computer Architecture

Major Assignment Mid-Term

Course Code: CSC-208

EDP Code: 102007051

Semester: Summer 2020

Q.1 Give answer to each of the following:

A. Draw the IBM zEnterprise EC12 Core layout and explain the function of each sub-area.

B. Discuss the IAS operation in detail.

C. What is embedded system? List differnt embeedded system used in everyday life.

D. Discuss different desktop applications that require the great power of contemporary microprocessor-based systems.

E. Discuss the techniques used in contemporary processors to increase speed.

F. Discuss the problems created due to increase in clockk speed and logic density of the processor.

G. Discuss the speedup of a program using multiple processors compared to a single processor using Amdahl's Law.

H. Discuss the multicore, MIC, and GPGPU in detail.

I. Discuss the QuickPath Interconnect (QPI) protocol layers.

J. Discuss the physical and Logical architecture of PCIe in detail.

Q.2 Write a detail note on each of the following:

A. Main structural components of a computer

B. Key characteristics of a planned computer family

C. Stored program computer

D. Moore's law

E. Instruction cycle state diagram

F. Classes of Interrupts

G. Bus Interconnection Scheme

Q.3 Differentiate each of the following:

A. Computer organization and computer architecture

B. RISC and CISC

C. Microprocessors and Microcontrollers

D. Cortex-A, Cortex-R, and Cortex-M

E. Program flow of control without interrupt and with interrupt

F. Disabled interrupt and nested interrupt processing

G. Programing in hardware and programming in software

Q.4 Solve each of the following:

A. Given the memory contents of the IAS computer shown below,

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB

a. Show the assembly language code for the program, starting at address 08A.

b. Explain what this program does.

B. On the IAS, what would the machine code instruction look like to load the contents of memory address 2 to the accumulator? How many trips to memory does the CPU need to make to complete this instruction during the instruction cycle?

C. A benchmark program is run on a 60 MHz processor. The executed program consists o f 104,000 instruction executions, with the instruction mix and clock cycle count given below. Determine the effective CPI, MIPS rate, and execution time for this program.

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	46,000	1
Data transfer	33,000	2
Floating point	16,000	2
Control transfer	9000	2

D. Consider the example in Section 2.5 for the calculation of average *CPI* and MIPS rate, which yielded the result of CPI = 2.24 and MIPS rate = 178. Now assume that the program can be executed in eight parallel tasks or threads with roughly equal number of instructions executed in each task. Execution is on an 8-core system with each core (processor) having the same performance as the single processor originally used. Coordination and synchronization between the parts adds an extra 25,000 instruction executions to each task. Assume the same instruction mix as in the example for each task, but increase the CPI for memory reference with cache miss to 12 cycles due to contention for memory.

a. Determine the average CPI.

b. Determine the corresponding MIPS rate.

c. Calculate the speedup factor.

d. Compare the actual speedup factor with the theoretical speedup factor determined by Amdahl's law.

E. The program execution of Figure 01 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

F. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: The first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?

b. Discuss the impact on the system speed if the microprocessor bus has:

1. 32-bit local address bus and a 16-bit local data bus, or
2. 16-bit local address bus and a 16-bit local data bus.

c. How many bits are needed for the program counter and the instruction register?

G. The Intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8086 uses a 16-bit bus that can transfer 2 bytes at a time, provided that the lower-order byte has an even address. However, the 8086 allows both even- and odd-aligned word operands. If an odd-aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it take to fetch the operands? Give the range of possible answers. Assume a clocking rate of 4 MHz and no wait states.

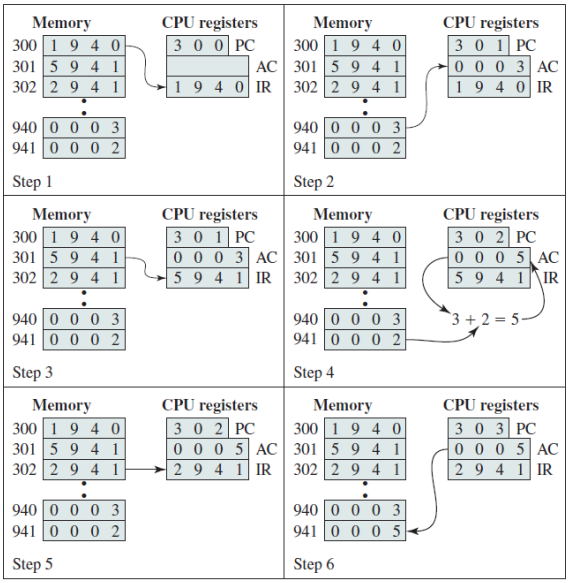

Figure 1 Example of Program Execution (contents of memory and registers in hexadecimal)