7-2 The Load Line

Figure 7-2*a* shows the CE connection discussed in Chap. 6. Given the values of R_B and β_{dc}, we can calculate collector current I_C and collector voltage V_{CE} using the methods of the preceding chapter.

Base Bias

The circuit of Fig. 7-2*a* is an example of **base bias,** which means setting up a *fixed value of base current.* For instance, if $R_B = 1\ \text{M}\Omega$, the base current is 14.3 μA (second approximation). Even with transistor replacements and temperature changes, the base current remains fixed at approximately 14.3 μA under all operating conditions.

If $\beta_{dc} = 100$ in Fig. 7-2*a*, the collector current is approximately 1.43 mA and the collector-emitter voltage is:

$$V_{CE} = V_{CC} - I_C R_C = 15\text{ V} - (1.43\text{ mA})(3\text{ k}\Omega) = 10.7\text{ V}$$

Therefore, the quiescent or Q point in Fig. 7-2*a* is:

$$I_C = 1.43\text{ mA} \qquad \text{and} \qquad V_{CE} = 10.7\text{ V}$$

Graphical Solution

We can also find the Q point using a graphical solution based on the transistor **load line,** a graph of I_C versus V_{CE}. In Fig. 7-2*a*, the collector-emitter voltage is given by:

$$V_{CE} = V_{CC} - I_C R_C$$

Solving for I_C gives:

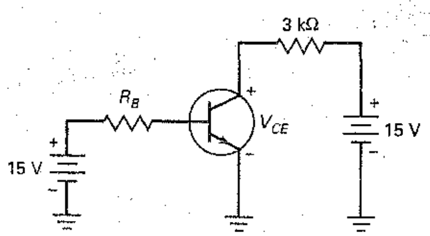
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{7-1}$$

If we graph this equation (I_C versus V_{CE}), we will get a straight line. This line is called the *load line* because it represents the effect of the load on I_C and V_{CE}.

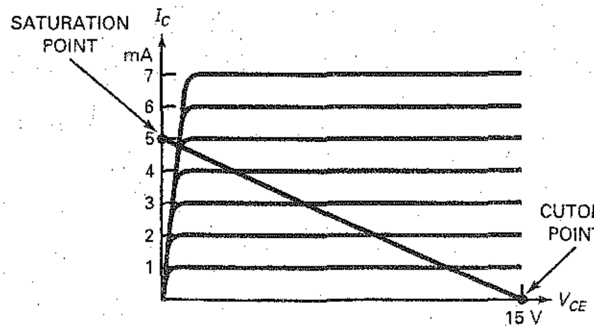
For instance, substituting the values of Fig. 7-2*a* into Eq. (7-1) gives:

$$I_C = \frac{15\text{ V} - V_{CE}}{3\text{ k}\Omega}$$

Figure 7-2 Base bias. (*a*) Circuit; (*b*) load line.



(*a*)



(*b*)

This equation is a linear equation; that is, its graph is a straight line. (*Note:* A *linear equation* is any equation that can be reduced to the standard form of $y = mx + b$.) If we graph the foregoing equation on top of the collector curves, we get Fig. 7-2*b*.

The ends of the load line are the easiest to find. When $V_{CE} = 0$ in the load-line equation (the foregoing equation):

$$I_C = \frac{15\text{ V}}{3\text{ k}\Omega} = 5\text{ mA}$$

The values, $I_C = 5$ mA and $V_{CE} = 0$, plot as the upper end of the load line in Fig. 7-2*b*.

When $I_C = 0$, the load-line equation gives:

$$0 = \frac{15\text{ V} - V_{CE}}{3\text{ k}\Omega}$$

or

$$V_{CE} = 15\text{ V}$$

The coordinates, $I_C = 0$ and $V_{CE} = 15$ V plot as the lower end of the load line in Fig. 7-2*b*.

Visual Summary of All Operating Points

Why is the load line useful? Because it contains every possible operating point for the circuit. Stated another way, when the base resistance varies from zero to infinity, it causes I_B to vary, which makes I_C and V_{CE} to vary over their entire ranges. If you plot the I_C and V_{CE} values for every possible I_B value, you will get the load line. Therefore, the load line is a visual summary of *all the possible transistor operating points.*

The Saturation Point

GOOD TO KNOW

When a transistor is saturated, further increases in base current produce no further increases in collector current.

When the base resistance is too small, there is too much collector current, and the collector-emitter voltage drops to approximately zero. In this case, the transistor goes into *saturation.* This means that the collector current has increased to its maximum possible value.

The **saturation point** is the point in Fig. 7-2*b* where the load line intersects the saturation region of the collector curves. Because the collector-emitter voltage V_{CE} at saturation is very small, the saturation point is almost touching the upper end of the load line. From now on, we will approximate the saturation point as the upper end of the load line, bearing in mind that there is a slight error.

The saturation point tells you the maximum possible collector current for the circuit. For instance, the transistor of Fig. 7-3*a* goes into saturation when the collector current is approximately 5 mA. At this current, V_{CE} has decreased to approximately zero.

There is an easy way to find the current at the saturation point. Visualize a short between the collector and emitter to get Fig. 7-3*b*. Then V_{CE} drops to zero. All the 15 V from the collector supply will be across the 3 kΩ. Therefore, the current is:

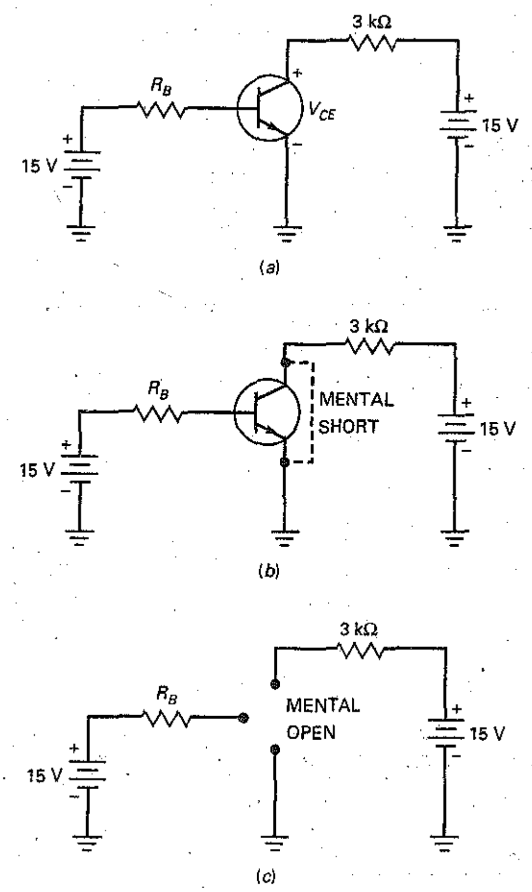
$$I_C = \frac{15\text{ V}}{3\text{ k}\Omega} = 5\text{ mA}$$

You can apply this "mental short" method to any base-biased circuit.

Here is the formula for the saturation current in base-biased circuits:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} \tag{7-2}$$

Figure 7-3 Finding the ends of the load line. (*a*) Circuit; (*b*) calculating collector saturation current; (*c*) calculating collector-emitter cutoff voltage.



This says that the maximum value of the collector current equals the collector supply voltage divided by the collector resistance. It is nothing more than Ohm's law applied to the collector resistor. Figure 7-3*b* is a visual reminder of this equation.

The Cutoff Point

The **cutoff point** is the point at which the load line intersects the cutoff region of the collector curves in Fig. 7-2*b*. Because the collector current at cutoff is very small, the cutoff point almost touches the lower end of the load line. From now on, we will approximate the cutoff point as the lower end of the load line.

The cutoff point tells you the maximum possible collector-emitter voltage for the circuit. In Fig. 7-3*a*, the maximum possible V_{CE} is approximately 15 V, the collector supply voltage.

There is a simple process for finding the cutoff voltage. Visualize the transistor of Fig. 7-3*a* as an open between the collector and the emitter (see Fig. 7-3*c*). Since there is no current through the collector resistor for this open condition, all the 15 V from the collector supply will appear between the collector-emitter terminals. Therefore, the voltage between the collector and the emitter will equal 15 V:

$$V_{CE(\text{cutoff})} = V_{CC} \tag{7-3}$$

GOOD TO KNOW

A transistor is cut off when its collector current is zero.

Example 7-1

IIII MultiSim

What are the saturation current and the cutoff voltage in Fig. 7-4*a*?

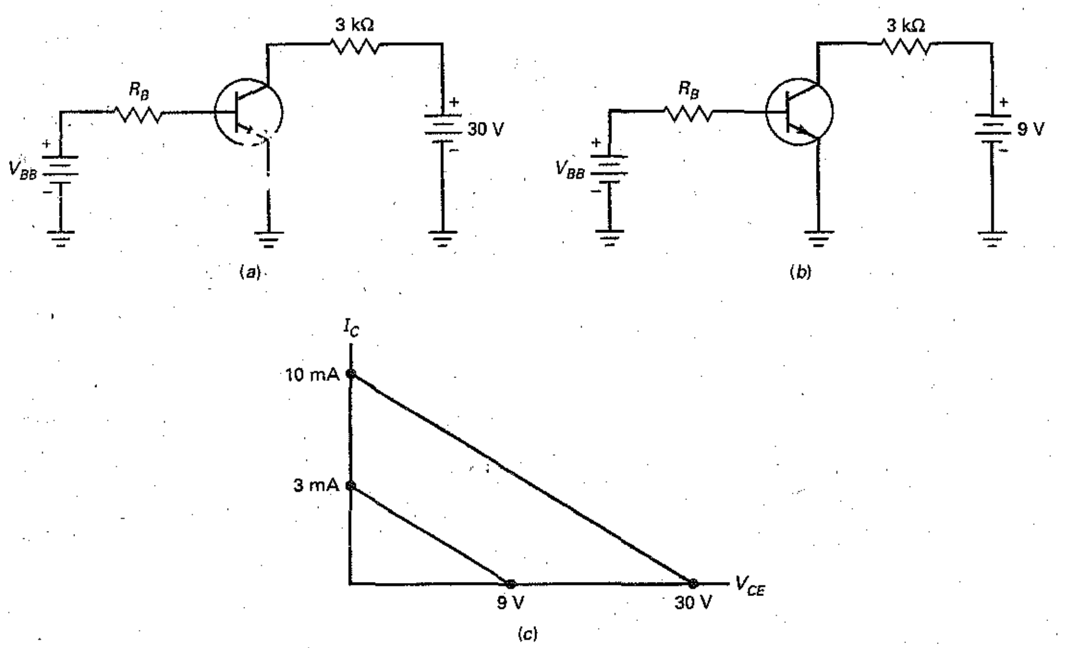
SOLUTION Visualize a short between the collector and emitter. Then:

$$I_{C(\text{sat})} = \frac{30\text{ V}}{3\text{ k}\Omega} = 10\text{ mA}$$

Next, visualize the collector-emitter terminals open. In this case:

$$V_{CE(\text{cutoff})} = 30\text{ V}$$

Figure 7-4 Load lines when collector resistance is the same. (*a*) With a collector supply of 30 V; (*b*) with a collector supply of 9 V; (*c*) load lines have same slope.



Example 7-2

Calculate the saturation and cutoff values for Fig. 7-4*b*. Draw the load lines for this and the preceding example.

SOLUTION With a mental short between the collector and emitter:

$$I_{C(\text{sat})} = \frac{9\text{ V}}{3\text{k}\Omega} = 3\text{ mA}$$

A mental open between the collector and emitter gives:

$$V_{CE(\text{cutoff})} = 9\text{ V}$$

Figure 7-4c shows the two load lines. Changing the collector supply voltage while keeping the same collector resistance produces two load lines of the same slope but with different saturation and cutoff values.

PRACTICE PROBLEM 7-2 Find the saturation current and cutoff voltage of Fig. 7-2a if the collector resistor is 2 kΩ and V_{CC} is 12 V.

Example 7-3

MultiSim

What are the saturation current and the cutoff voltage in Fig. 7-5a?

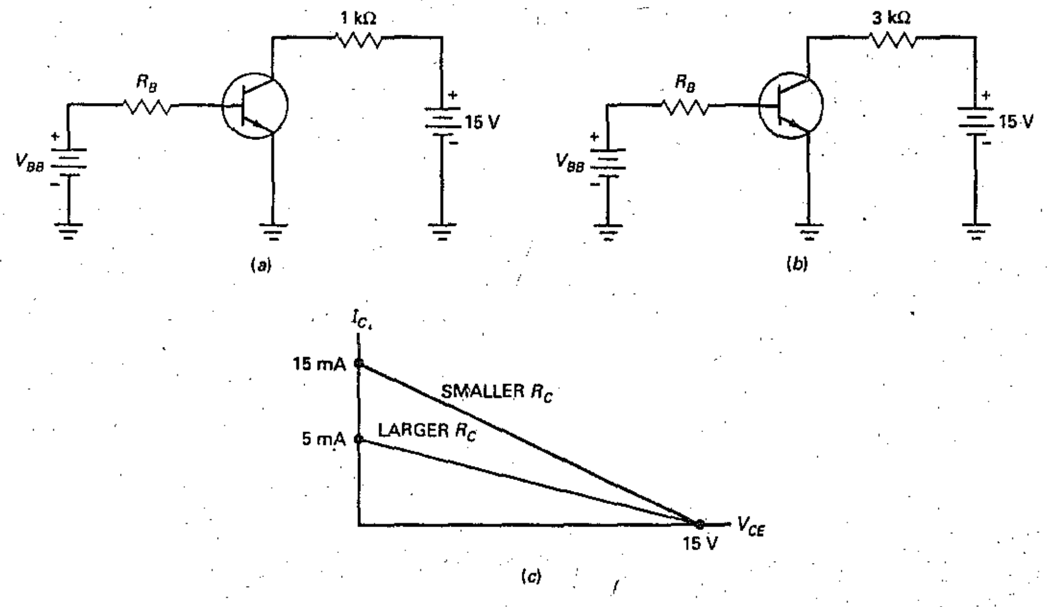
SOLUTION The saturation current is:

$$I_{C(\text{sat})} = \frac{15\text{ V}}{1\text{ k}\Omega} = 15\text{ mA}$$

The cutoff voltage is:

$$V_{CE(\text{cutoff})} = 15\text{ V}$$

Figure 7-5 Load lines when collector voltage is the same. (a) With a collector resistance of 1 kΩ; (b) with a collector resistance of 3 kΩ; (c) smaller R_C produces steeper slope.



Example 7-4

Calculate the saturation and cutoff values for Fig. 7-5b. Then, compare the load lines for this and the preceding example.

SOLUTION The calculations are as follows:

$$I_{C(\text{sat})} = \frac{15\text{ V}}{3\text{ k}\Omega} = 5\text{ mA}$$

and

$V_{CE(\text{cutoff})} = 15\ \text{V}$

Figure 7-5*c* shows the two load lines. Changing the collector resistor with the same collector supply voltage produces load lines of different slopes but the same cutoff values. Also, notice that a smaller collector resistance produces a larger slope (steeper or closer to vertical). This happens because the slope of the load line is equal to the reciprocal of the collector resistance:

$$\text{Slope} = \frac{1}{R_C}$$

PRACTICE PROBLEM 7-4 Using Fig. 7-5*b*, what happens to the circuit's load line if the collector resistor is changed to 5 kΩ?

7-3 The Operating Point

Every transistor circuit has a load line. Given any circuit, work out the saturation current and the cutoff voltage. These values are plotted on the vertical and horizontal axes. Then draw a line through these two points to get the load line.

Plotting the *Q* Point

Figure 7-6*a* shows a base-biased circuit with a base resistance of 500 kΩ. We get the saturation current and cutoff voltage by the process given earlier. First, visualize a short across the collector-emitter terminals. Then all the collector supply voltage appears across the collector resistor, which means that the saturation current is 5 mA. Second, visualize the collector-emitter terminals open. Then there is no current, and all the supply voltage appears across the collector-emitter terminals, which means that the cutoff voltage is 15 V. If we plot the saturation current and cutoff voltage, we can draw the load line shown in Fig. 7-6*b*.

Figure 7-6 Calculating the *Q* point. (*a*) Circuit; (*b*) change in current gain changes *Q* point.