8

Field-Effect Transistors (FETs)

CHAPTER OUTLINE

CHAPTER OBJECTIVES

- Discuss the JFET and how it differs from the BJT
- Discuss, define, and apply JFET characteristics and parameters
- Discuss and analyze JFET biasing
- Discuss the ohmic region on a JFET characteristic curve
- Explain the operation of MOSFETs
- Discuss and apply MOSFET parameters
- Describe and analyze MOSFET bias circuits
- Discuss the IGBT
- Troubleshoot FET circuits

KEY TERMS

- JFET
- Drain
- Source
- Gate
- Pinch-off voltage
- Transconductance
- Ohmic region
- MOSFET
- Depletion
- Enhancement
- IGBT

APPLICATION ACTIVITY PREVIEW

The Application Activity involves the electronic control circuits for a waste water treatment system. In particular, you will focus on the application of field-effect transistors in the sensing circuits for chemical measurements.

VISIT THE COMPANION WEBSITE

Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

BJTs (bipolar junction transistors) were covered in previous chapters. Now we will discuss the second major type of transistor, the FET (field-effect transistor). **FETs** are unipolar devices because, unlike BJTs that use both electron and hole current, they operate only with one type of charge carrier. The two main types of FETs are the junction field-effect transistor (JFET) and the metal oxide semiconductor field-effect transistor (MOSFET). The term *field-effect* relates to the depletion region formed in the channel of a FET as a result of a voltage applied on one of its terminals (gate).

Recall that a BJT is a current-controlled device; that is, the base current controls the amount of collector current. A FET is different. It is a voltage-controlled device, where the voltage between two of the terminals (gate and source) controls the current through the device. A major advantage of FETs is their very high input resistance. Because of their nonlinear characteristics, they are generally not as widely used in amplifiers as BJTs except where very high input impedances are required. However, FETs are the preferred device in low-voltage switching applications because they are generally faster than BJTs when turned on and off. The IGBT is generally used in high-voltage switching applications.

8–1 THE JFET

The **JFET** (junction field-effect transistor) is a type of FET that operates with a reverse-biased *pn* junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, *n* channel or *p* channel.

After completing this section, you should be able to

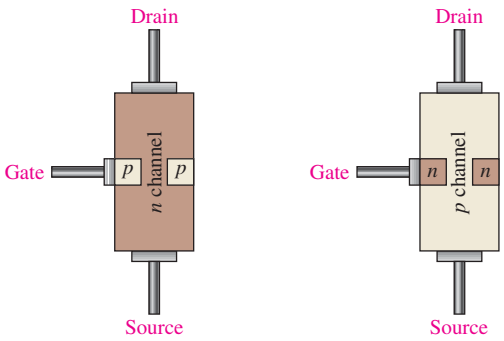
- **Discuss the JFET and how it differs from the BJT**
- Describe the basic structure of *n*-channel and *p*-channel JFETs
  - Name the terminals
  - Explain a channel
- Explain the basic operation of a JFET
- Identify JFET schematic symbols

Basic Structure

Figure 8–1(a) shows the basic structure of an *n*-channel JFET (junction field-effect transistor). Wire leads are connected to each end of the *n*-channel; the **drain** is at the upper end, and the **source** is at the lower end. Two *p*-type regions are diffused in the *n*-type material to form a **channel,** and both *p*-type regions are connected to the **gate** lead. For simplicity, the gate lead is shown connected to only one of the *p* regions. A *p*-channel JFET is shown in Figure 8–1(b).

HISTORY NOTE

In 1952, Ian Ross and George Dacey succeeded in making a unipolar device with a structure similar to today's JFET.



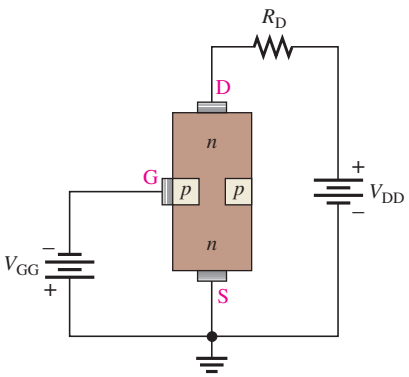
(a) *n* channel (b) *p* channel

◀ FIGURE 8–1

A representation of the basic structure of the two types of JFET.

Basic Operation

To illustrate the operation of a JFET, Figure 8–2 shows dc bias voltages applied to an *n*-channel device. V_{DD} provides a drain-to-source voltage and supplies current from



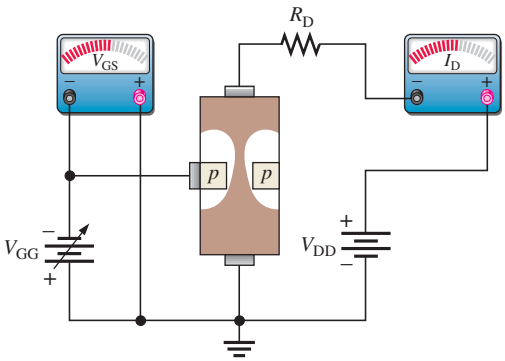
◀ FIGURE 8–2

A biased *n*-channel JFET.

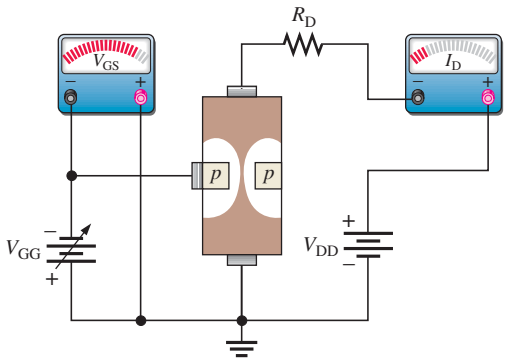
drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown.

The JFET is always operated with the gate-source pn junction reverse-biased. Reverse-biasing of the gate-source junction with a negative gate voltage produces a depletion region along the *pn* junction, which extends into the *n* channel and thus increases its resistance by restricting the channel width.

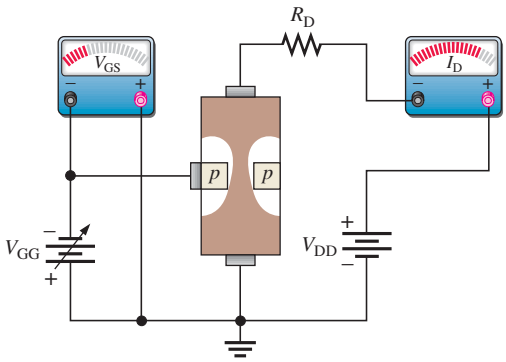
The channel width and thus the channel resistance can be controlled by varying the gate voltage, thereby controlling the amount of drain current, I_D. Figure 8–3 illustrates this concept. The white areas represent the depletion region created by the reverse bias. It is wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is greater than that between the gate and the source. We will discuss JFET characteristic curves and some parameters in Section 8–2.



(a) JFET biased for conduction



(b) Greater V_{GG} narrows the channel (between the white areas) which increases the resistance of the channel and decreases I_D.



(c) Less V_{GG} widens the channel (between the white areas) which decreases the resistance of the channel and increases I_D.

▲ **FIGURE 8–3**

Effects of V_{GS} on channel width, resistance, and drain current ($V_{GG} = V_{GS}$).

JFET Symbols

The schematic symbols for both *n*-channel and *p*-channel JFETs are shown in Figure 8–4. Notice that the arrow on the gate points "in" for *n* channel and "out" for *p* channel.

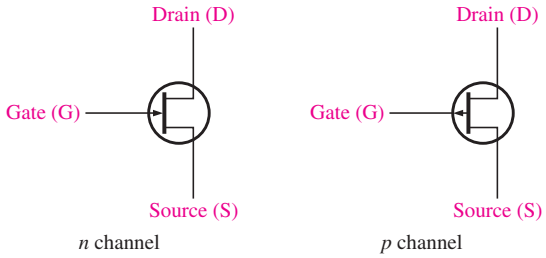


FIGURE 8–4
JFET schematic symbols.

SECTION 8–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. Name the three terminals of a JFET.
2. Does an *n*-channel JFET require a positive or negative value for V_{GS}?
3. How is the drain current controlled in a JFET?

8–2 JFET Characteristics and Parameters

The JFET operates as a voltage-controlled, constant-current device. Cutoff and pinch-off as well as JFET transfer characteristics are covered in this section.

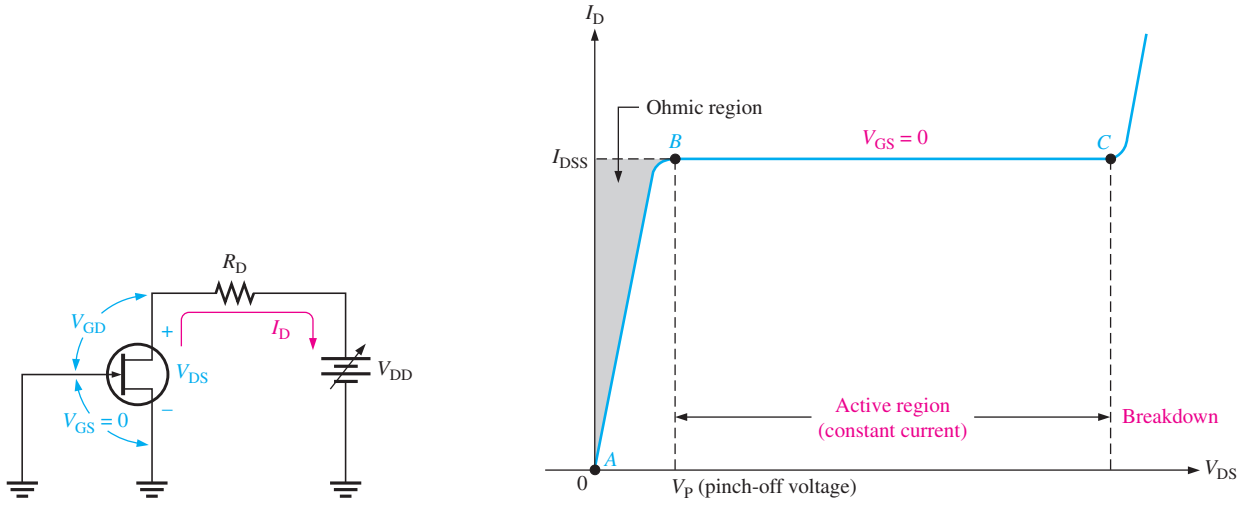
After completing this section, you should be able to

- **Discuss, define, and apply JFET characteristics and parameters**
- Discuss the drain characteristic curve
  - Identify the ohmic, active, and breakdown regions of the curve
- Define *pinch-off voltage*
- Discuss breakdown
- Explain how gate-to-source voltage controls the drain current
- Discuss the cutoff voltage
- Compare pinch-off and cutoff
- Explain the JFET universal transfer characteristic
  - Calculate the drain current using the transfer characteristic equation
  - Interpret a JFET datasheet
- Discuss JFET forward transconductance
  - Define *transconductance* ◆ Calculate forward transconductance
- Discuss JFET input resistance and capacitance
- Determine the ac drain-to-source resistance

Drain Characteristic Curve

Consider the case when the gate-to-source voltage is zero ($V_{GS} = 0$ V). This is produced by shorting the gate to the source, as in Figure 8–5(a) where both are grounded. As V_{DD} (and thus V_{DS}) is increased from 0 V, I_D will increase proportionally, as shown in the graph of Figure 8–5(b) between points *A* and *B*. In this area, the channel resistance is essentially constant because the depletion region is not large enough to have significant effect. This is called the *ohmic region* because V_{DS} and I_D are related by Ohm's law. (Ohmic region is discussed further in Section 8–4.)

At point *B* in Figure 8–5(b), the curve levels off and enters the active region where I_D becomes essentially constant. As V_{DS} increases from point *B* to point *C*, the reverse-bias



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

(b) Drain characteristic

▲ FIGURE 8–5

The drain characteristic curve of a JFET for $V_{GS} = 0$ showing pinch-off voltage.

voltage from gate to drain (V_{GD}) produces a depletion region large enough to offset the increase in V_{DS}, thus keeping I_D relatively constant.

Pinch-Off Voltage For $V_{GS} = 0$ V, the value of V_{DS} at which I_D becomes essentially constant (point *B* on the curve in Figure 8–5(b)) is the **pinch-off voltage**, V_P. For a given JFET, V_P has a fixed value. As you can see, a continued increase in V_{DS} above the pinch-off voltage produces an almost constant drain current. This value of drain current is I_{DSS} (*D*rain to *S*ource current with gate *S*horted) and is always specified on JFET datasheets. I_{DSS} is the *maximum* drain current that a specific JFET can produce regardless of the external circuit, and it is always specified for the condition, $V_{GS} = 0$ V.

Breakdown As shown in the graph in Figure 8–5(b), **breakdown** occurs at point *C* when I_D begins to increase very rapidly with any further increase in V_{DS}. Breakdown can result in irreversible damage to the device, so JFETs are always operated below breakdown and within the active region (constant current) (between points *B* and *C* on the graph). The JFET action that produces the drain characteristic curve to the point of breakdown for $V_{GS} = 0$ V is illustrated in Figure 8–6.

V_{GS} Controls I_D

Let's connect a bias voltage, V_{GG}, from gate to source as shown in Figure 8–7(a). As V_{GS} is set to increasingly more negative values by adjusting V_{GG}, a family of drain characteristic curves is produced, as shown in Figure 8–7(b). Notice that I_D decreases as the magnitude of V_{GS} is increased to larger negative values because of the narrowing of the channel. Also notice that, for each increase in V_{GS}, the JFET reaches pinch-off (where constant current begins) at values of V_{DS} less than V_P. The term *pinch-off* is not the same as pinch-off voltage, V_p. Therefore, the amount of drain current is controlled by V_{GS}, as illustrated in Figure 8–8.

Cutoff Voltage

The value of V_{GS} that makes I_D approximately zero is the **cutoff voltage,** $V_{GS(off)}$, as shown in Figure 8–8(d). The JFET must be operated between $V_{GS} = 0$ V and $V_{GS(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.