Digital Logic & Design/Digital Systems

Programs: BS(CS)/BS(SE)/BS(TELC)
Course Codes: CSC-201/ SEC-201/TSC-201
EDP Codes: 102007016
Instructor: Muhammad Amin
Examination: Final Term
Semester: Summer 2020
Date: Sep. 26, 2020
Timing: 3:00 pm – 7:00 pm

Question No.	Q.1	Q.2	Q.3	Q.4	Q.5	Q.6	Q.7	Q.8	Q.9	
Total Marks	5	5	5	5	6	6	6	6	6	50

Note: Attempt all questions.

Q.1 Draw the logic circuit using the input (A, B, C, D) and output (X) waveforms in Figure 01.

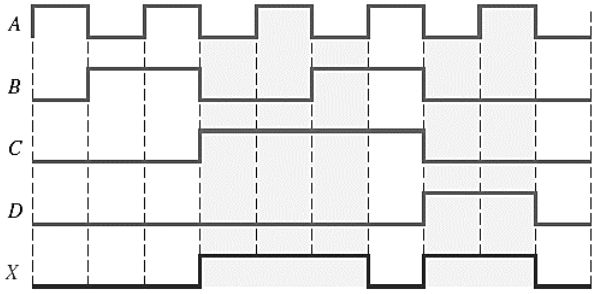


FIGURE 01

Q.2 For the 4-input multiplexer, data inputs are given as:

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find the output Y if the select inputs are given as:

a) $S_0 = 1$, $S_1 = 0$

b) $S_0 = 0$, $S_1 = 1$

c) $S_0 = 1$, $S_1 = 1$

d) $S_0 = 0$, $S_1 = 0$

Q.3 For the circuit in Figure 02, assume the inputs are $\overline{Add}/Subt. = 1$, $A = 1010$, and $B = 1101$. What is the output?

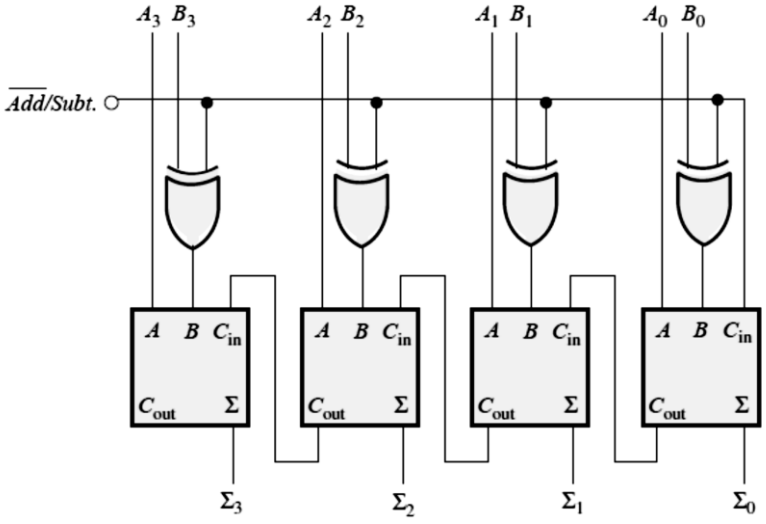


FIGURE 02

Q.4 Determine the A = B, A > B, and A < B outputs for the input numbers shown on the comparator in Figure 03.

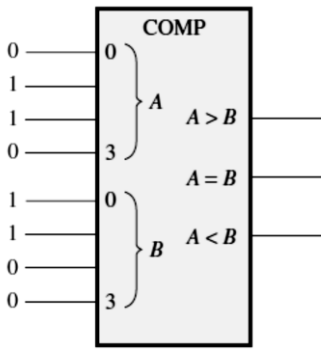


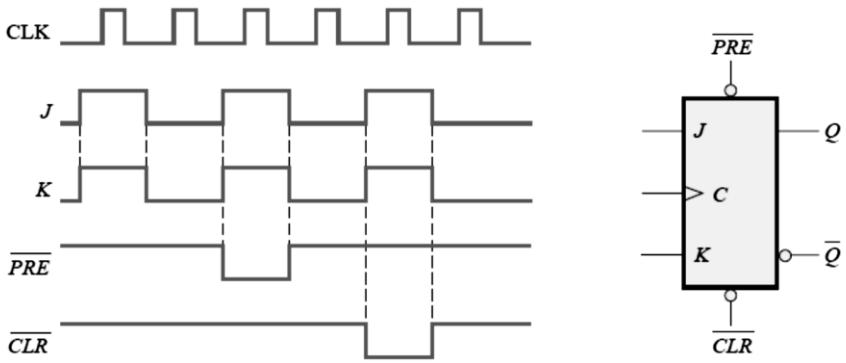
FIGURE 03

Q.5 Show the logic required to convert a 4-bit Gray code to binary and use that logic to convert the following Gray code words to binary: 1011

Q.6 Draw and explain the logic diagram for 4-bit active low decoder.

Q.7 Draw and explain the logic diagram for frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)

Q.8 Determine the Q waveform relative to the clock if the signals shown in Figure 04 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.



Q----------?

FIGURE 04

Q.9 Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

*********End of Exam*********