Department of Electrical Engineering
Assignment
Date: 24/06/2020

Course Details

Course Title: Digital Logic Design (B Tech) **Module:** _____
Instructor: _____ **Total Marks:** 50

Student Details

Name: _____ **Student ID:** _____

Note: Draw neat diagrams where necessary. Assume missing details if required.

Q1.	**Simplify the 4 variables expression in SOP term using K Map:** $\overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\,C\,\overline{D} + A\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,C\,\overline{D}$	**Marks 10**
Q2.	**Simplify 4 variables expression in POS term using K Map:** **F (A, B, C, D) =** $\text{Maxterms at}(2, 4, 5, 7, 9, 10, 11, 13, 15)$ **with don't care at (0, 8, 12)**	**Marks 10**
Q3.	**Implement the function F (A, B, C, D) = Σ (1, 2, 4, 5, 7, 9, 12, 14) using MUX.**	**Marks 10**
Q4.	**Design a combinational circuit with three inputs A, B, and C, and three outputs X, Y, and Z. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.**	**Marks 10**
Q5.	**Draw the logic diagram of a 2 to 4 line decoder using NOR gates only. Also Include an enable input.**	**Marks 10**