Digital Logic & Design (Lab)

Examination: Lab
Instructor: Muhammad Amin
Program: BS(SE)
Course Codes: CSC-201
EDP Codes: 102002016
Semester: Spring 2020
Date: July 8, 2020
Timing: 11:00am to 6:00pm

Note: Use MultiSim to design the follwing circuits. Use truth tables where necessary.

Q.1 Design and verify the logic circuit for the following:

(a) Half adder using logic gates

(b) Half-subtractor using logic gate

(c) J K Flip flop

(d) Serial in-serial Out shift register

(e) Synchronous BCD Counter