

Digital Logic & Design (Theory)

Final-Term Assignment

Instructor: Muhammad Amin

Program: BS (CS)

Course Codes: CSC-201

EDP Codes: 102002077

Semester: Spring 2020

Total Marks: 50

Date: June 26, 2020

Timing: 12:00pm to 6:00pm

Note: Attempt all questions. Use examples and diagrams where necessary.

- Q.1** Draw and explain the logic diagram for each of the following:
- A circuit for adding or subtracting two 4-bit numbers
 - 4-bit active low decoder
 - Decimal to BCD encoder
 - Frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)
- Q.2** For the 4-input multiplexer, data inputs are given as:
 $D_0 = 0, D_1 = 1, D_2 = 0, D_3 = 1$
Find the output Y if the select inputs are given as:
- $S_0 = 1, S_1 = 0$
 - $S_0 = 0, S_1 = 1$
 - $S_0 = 1, S_1 = 1$
 - $S_0 = 0, S_1 = 0$
- Q.3** Timing diagram in Figure 01 shows inputs to a 9-bit parity checker. Draw the Σ Even and Σ Odd output for the even parity checking.
- Q.4** The waveforms in Figure 02 are applied to the J, K, CLK, \overline{PRE} , and \overline{CLR} inputs as indicated. Determine the Q output, if the flip-flop is initially RESET.
- Q.5** Use the waveforms in Figure 03 to draw the timing diagram for the parallel outputs (Q_1, Q_2, Q_3, Q_4) for the shift register. Assume that register is initially cleared.
- Q.6** Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

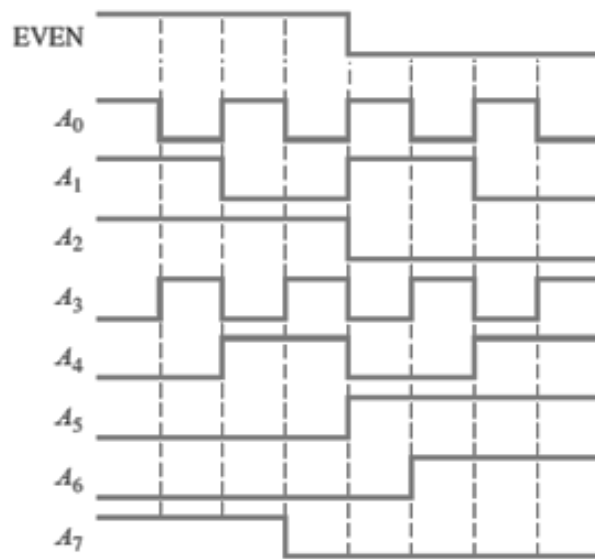


Figure 01

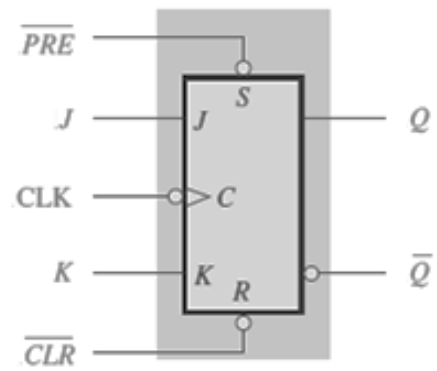
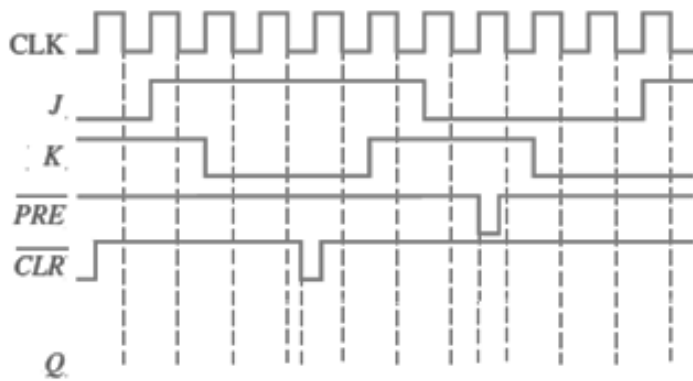


Figure 02

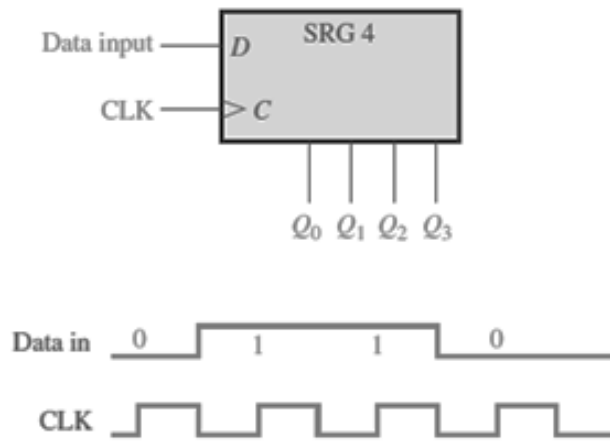


Figure 03