14–1 The Depletion-Mode MOSFET

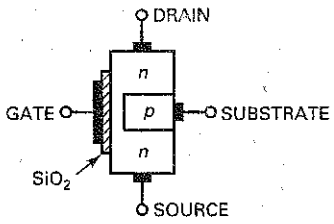
Figure 14-1 shows a **depletion-mode MOSFET,** a piece of n material with an insulated gate on the left and a p region on the right. The p region is called the **substrate.** Electrons flowing from source to drain must pass through the narrow channel between the gate and the p substrate.

A thin layer of silicon dioxide (SiO_2) is deposited on the left side of the channel. Silicon dioxide is the same as glass, which is an insulator. In a MOSFET, the gate is metallic. Because the metallic gate is insulated from the channel, negligible gate current flows even when the gate voltage is positive.

Figure 14-2*a* shows a depletion-mode MOSFET with a negative gate voltage. The V_{DD} supply forces free electrons to flow from source to drain. These electrons flow through the narrow channel on the left of the p substrate. As with a JFET, the gate voltage controls the width of the channel. The more negative the gate voltage, the smaller the drain current. When the gate voltage is negative enough, the drain current is cut off. Therefore, the operation of a depletion-mode MOSFET is similar to that of a JFET when V_{GS} is negative.

Since the gate is insulated, we can also use a positive input voltage, as shown in Fig. 14-2*b*. The positive gate voltage increases the number of free electrons flowing through the channel. The more positive the gate voltage, the greater the conduction from source to drain.

Figure 14–1 Depletion-mode MOSFET.



GOOD TO KNOW

Like a JFET, a depletion-mode MOSFET is considered a normally on device. This is because both devices have drain current when $V_{GS} = 0$ V. Recall that for a JFET, I_{DSS} is the maximum possible drain current. With a depletion-mode MOSFET, the drain current can exceed I_{DSS} if the gate voltage is of the correct polarity to increase the number of charge carriers in the channel. For an n-channel D-MOSFET, I_D is greater than I_{DSS} when V_{GS} is positive.

14–2 D-MOSFET Curves

Figure 14-3*a* shows the set of drain curves for a typical n-channel, depletion-mode MOSFET. Notice that the curves above $V_{GS} = 0$ are positive and the curves below $V_{GS} = 0$ are negative. As with a JFET, the bottom curve is for $V_{GS} = V_{GS(off)}$ and the drain current will be approximately zero. As shown, when $V_{GS} = 0$ V, the drain current will equal I_{DSS}. This demonstrates that the depletion-mode MOSFET, or D-MOSFET, is a *normally on* device. When V_{GS} is made negative, the drain current will be reduced. In contrast to an n-channel JFET, the n-channel D-MOSFET can have V_{GS} made positive and still function properly. This is because there is no pn junction to become forward biased. When V_{GS} becomes positive, I_D will increase following the square-law equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \tag{14-1}$$

Figure 14–2 (*a*) D-MOSFET with negative gate; (*b*) D-MOSFET with positive gate.

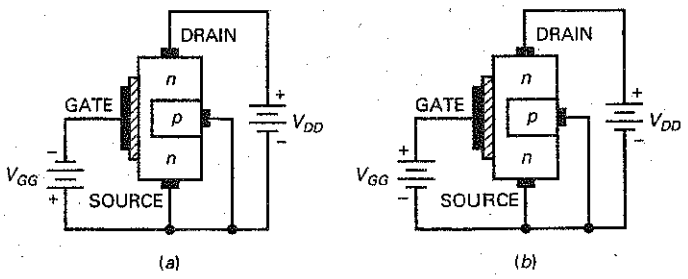
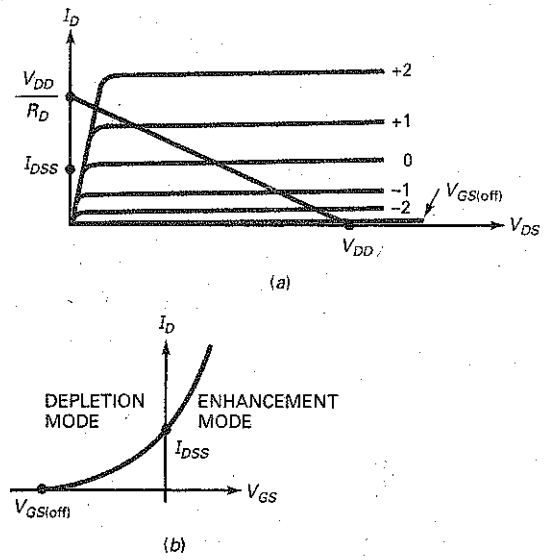


Figure 14–3 An *n*-channel, depletion-mode MOSFETs: (*a*) Drain curves; (*b*) transconductance curve.

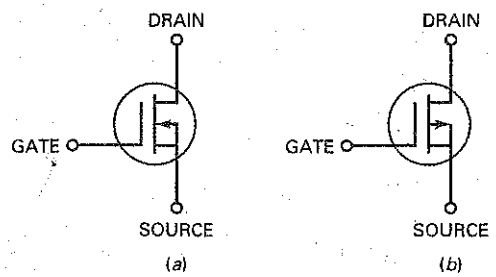


When V_{GS} is negative, the D-MOSFET is operating in the depletion mode. When V_{GS} is positive, the D-MOSFET is operating in the enhancement mode. Like the JFET, the D-MOSFET curves display an ohmic region, a current-source region, and a cutoff region.

Figure 14-3*b* is the transconductance curve for a D-MOSFET. Again, I_{DSS} is the drain current with the gate shorted to the source. I_{DSS} is no longer the maximum possible drain current. The parabolic transconductance curve follows the same square-law relation that exists with a JFET. As a result, the analysis of a depletion-mode MOSFET is almost identical to that of a JFET circuit. The major difference is enabling V_{GS} to be either negative or positive.

There is also a *p*-channel D-MOSFET. It consists of a drain-to-source *p*-channel, along with a *n*-type substrate. Once again, the gate is insulated from the channel. The action of a *p*-channel MOSFET is complementary to the *n*-channel MOSFET. The schematic symbols for both *n*-channel and *p*-channel D-MOSFETs are shown in Fig. 14-4.

Figure 14–4 D-MOSFET schematic symbols: (*a*) *n*-channel; (*b*) *p*-channel.



Example 14–1

A D-MOSFET has the values $V_{GS(off)} = -3$ V and $I_{DSS} = 6$ mA. What will the drain current equal when V_{GS} equals -1 V, -2 V, 0 V, $+1$ V, and $+2$ V?

SOLUTION Following the square-law equation (14-1), when

$V_{GS} = -1$ V $\quad I_D = 2.67$ mA

$V_{GS} = -2$ V $\quad I_D = 0.667$ mA

$V_{GS} = 0$ V $\quad I_D = 6$ mA

$V_{GS} = +1$ V $\quad I_D = 10.7$ mA

$V_{GS} = +2$ V $\quad I_D = 16.7$ mA

PRACTICE PROBLEM 14–1 Repeat example 14-1 using the values $V_{GS(off)} = -4$ V and $I_{DSS} = 4$ mA.

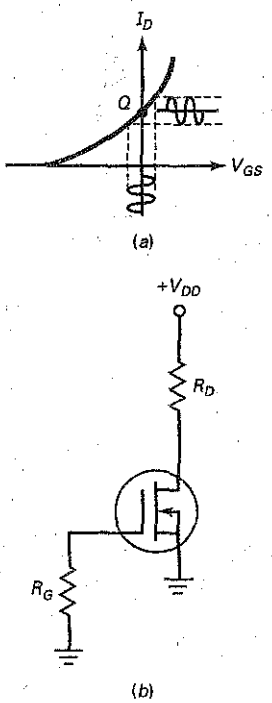
14–3 Depletion-Mode MOSFET Amplifiers

A depletion-mode MOSFET is unique because it can operate with a positive or a negative gate voltage. Because of this, we can set its Q point at $V_{GS} = 0$ V, as shown in Fig. 14-5*a*. When the input signal goes positive, it increases I_D above I_{DSS}. When the input signal goes negative, it decreases I_D below I_{DSS}. Because there is no *pn* junction to forward bias, the input resistance of the MOSFET remains very high. Being able to use zero V_{GS} allows us to build the very simple bias circuit of Fig. 14-5*b*. Because I_G is zero, $V_{GS} = 0$ V and $I_D = I_{DSS}$. The drain voltage is:

$$V_{DS} = V_{DD} - I_{DSS} R_D \tag{14-2}$$

Due to the fact that a D-MOSFET is a normally on device, it is also possible to use self-bias by adding a source resistor. The operation becomes the same as a self-biased JFET circuit.

Figure 14–5 Zero-bias.



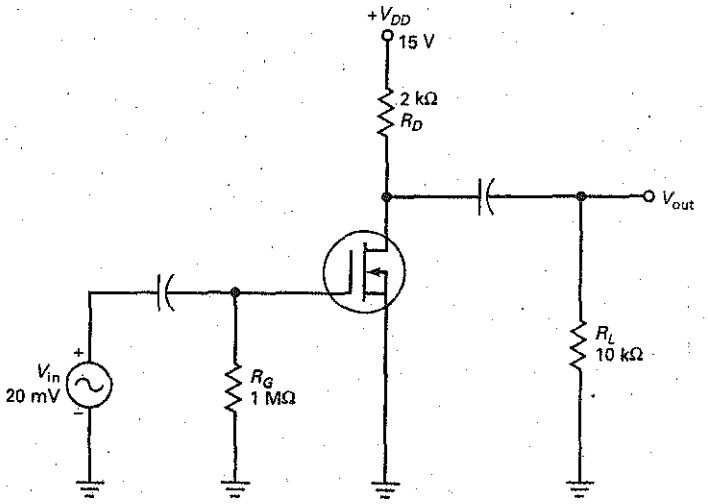
Example 14–2

The D-MOSFET amplifier shown in Fig. 14-6 has $V_{GS(off)} = -2$ V, $I_{DSS} = 4$ mA, and $g_{mo} = 2000$ μS. What is the circuit's output voltage?

SOLUTION With the source grounded, $V_{GS} = 0$ V and $I_D = 4$ mA.

$V_{DS} = 15 \text{ V} - (4 \text{ mA})(2 \text{ k}\Omega) = 7 \text{ V}$

Figure 14–6 D-MOSFET amplifier.



Since $V_{GS} = 0$ V, $gm = g_{mo} = 2000$ μS.
The amplifier's voltage gain is found by:

$$A_V = g_m r_d$$

The ac drain resistance is equal to:

$$r_d = R_D \| R_L = 2\text{ K} \| 10\text{ K} = 1.76\text{ k}\Omega$$

and A_V is:

$$A_V = (2000\ \mu\text{S})(1.67\ \text{k}\Omega) = 3.34$$

Therefore,

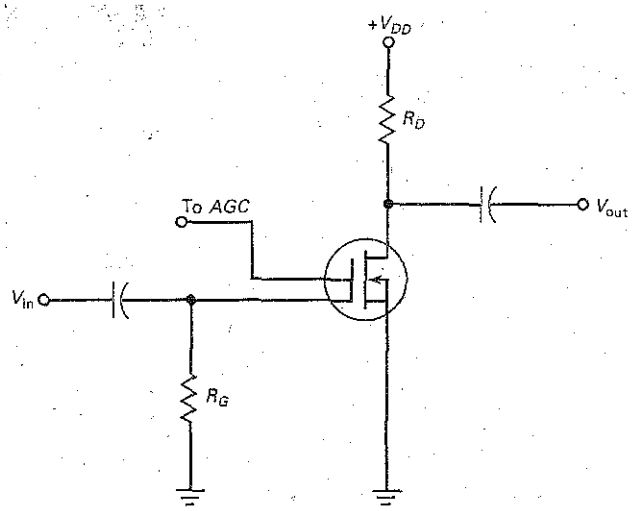
$$V_{out} = (V_{in})(A_V) = (20\text{ mV})(3.34) = 66.8\text{ mV}$$

PRACTICE PROBLEM 14–2 In Fig. 14-6, if the MOSFET's g_{mo} value is 3000 μS, what is the value of V_{out}?

As shown by Example 14-2, the D-MOSFET has a relatively low voltage gain. One of the major advantages of this device is its extremely high input resistance. This allows us to use this device when circuit loading could be a problem. Also, MOSFETs have excellent low-noise properties. This is a definite advantage for any stage near the front end of a system where the signal is weak. This is very common in many types of electronic communications circuits.

Some D-MOSFETs, as shown in Fig. 14-7, are dual-gate devices. One gate can serve as the input signal point, while the other gate can be connected to an automatic gain control dc voltage. This allows the voltage gain of the MOSFET to be controlled and varied depending on the input signal strength.

Figure 14–7 Dual-gate MOSFET.



14–4 The Enhancement-Mode MOSFET

The depletion-mode MOSFET was part of the evolution toward the **enhancement-mode MOSFET,** abbreviated *E-MOSFET.* Without the E-MOSFET, the personal computers that are now so widespread would not exist.

The Basic Idea

Figure 14-8*a* shows an E-MOSFET. The *p* substrate now extends all the way to the silicon dioxide. As you can see, there no longer is an *n* channel between the source and the drain. How does an E-MOSFET work? Figure 14-8*b* shows normal biasing polarities. When the gate voltage is zero, the current between source and drain is zero. For this reason, an E-MOSFET is *normally off* when the gate voltage is zero.

The only way to get current is with a positive gate voltage. When the gate is positive, it attracts free electrons into the *p* region. The free electrons recombine with the holes next to the silicon dioxide. When the gate voltage is positive enough, all the holes touching the silicon dioxide are filled and free electrons begin to flow from the source to the drain. The effect is the same as creating a thin layer of *n*-type material next to the silicon dioxide. This thin conducting layer is

Figure 14–8 Enhancement-mode MOSFET: (*a*) Unbiased; (*b*) biased.