Computer Architecture
Course Code: CSC-208
EDP Code: 102007051
Program: BS(CS)
Instructor: Muhammad Amin
Examination: Mid Term
Semester: Summer 2020
Duration: 04 Hours
Total Marks: 30
Date: Aug. 21, 2020
Time: 09:00am

Note: Attempt all questions. Use examples and diagram where necessary.

Q.1 Give answer to each of the following: (2 x 4 = 08)

a. Discuss the techniques used in contemporary processors to increase speed.

b. Discuss the speedup of a program using multiple processors compared to a single processor using Amdahl's Law.

c. Discuss the QuickPath Interconnect (QPI) protocol layers.

d. Discuss the physical and Logical architecture of PCIe in detail.

Q.2 Write a note on each of the following: (2 x 4 = 08)

a. Consequences of Moore's law

b. Key characteristics of a planned computer family

c. Instruction Cycle State Diagram

d. Classes of Interrupts

Q.3 Differentiate each of the following: (2 x 3 = 06)

a. Cortex-A, Cortex-R, and Cortex-M

b. Multicore, MIC, and GPGPU

c. Disabled interrupt and nested interrupt processing

Q.4 a. Figure 01 shows the IBM zEnterprise EC12 Core layout. Briefly explain the function of each sub-area. (03)

b. Discuss the IAS operation using the flowchart in Figure 02. (02)

Q.5 A benchmark program is run on a 60 MHz processor. The executed program consists of 104,000 instruction executions, with the instruction mix and clock cycle count given below. Determine the effective CPI, MIPS rate, and execution time for this program. (03)

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	46,000	1
Data transfer	33,000	2
Floating point	16,000	2
Control transfer	9000	2

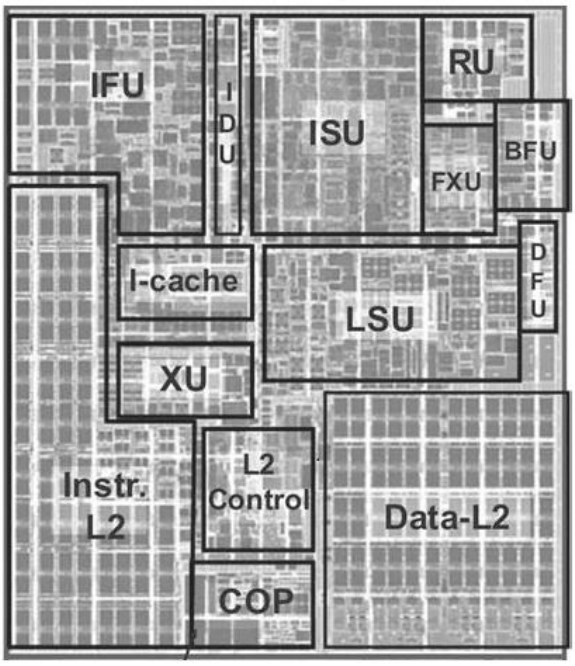

Figure 01

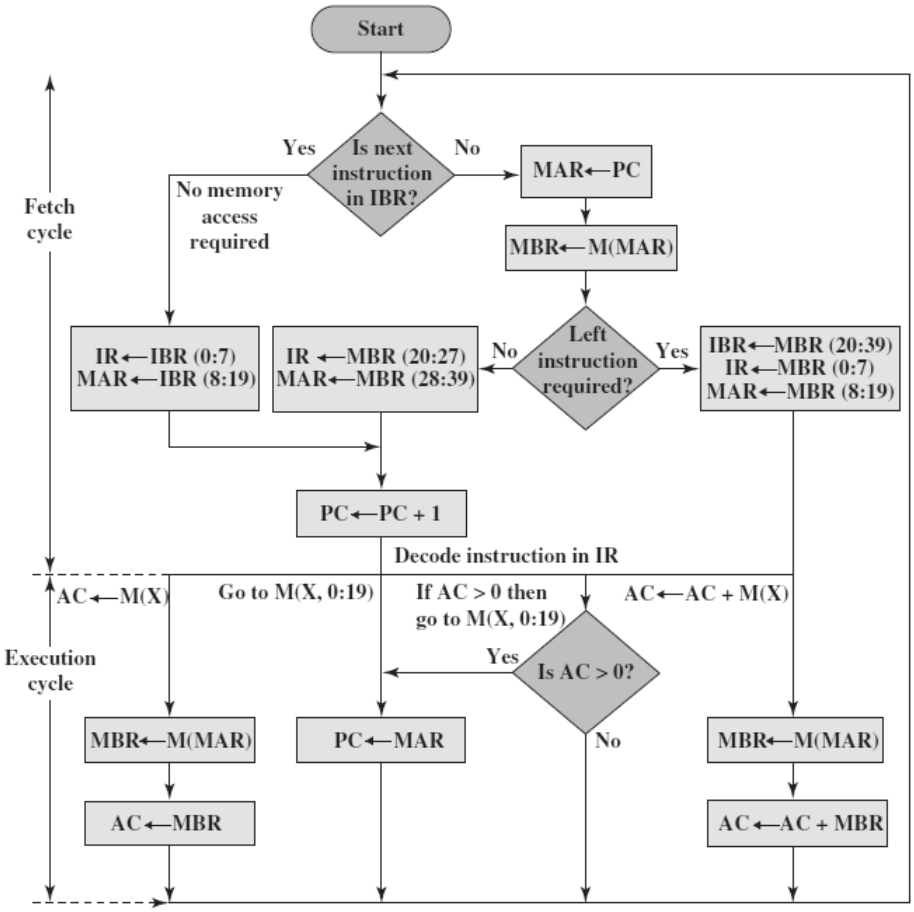

Figure 02