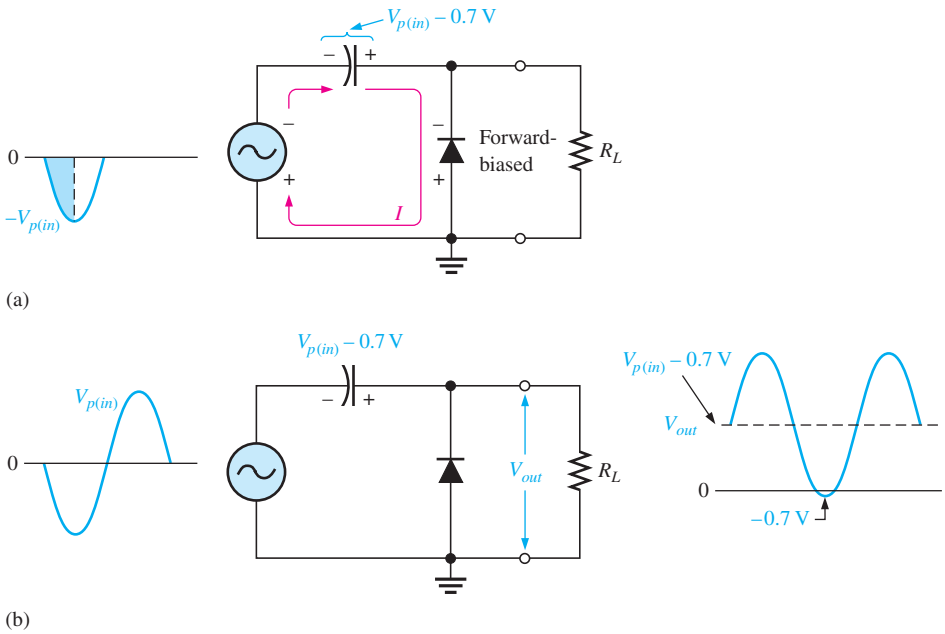
Diode Clampers

A clamper adds a dc level to an ac voltage. **Clampers** are sometimes known as *dc restorers*. Figure 2–63 shows a diode clamper that inserts a positive dc level in the output waveform. The operation of this circuit can be seen by considering the first negative half-cycle of the input voltage. When the input voltage initially goes negative, the diode is forward-biased, allowing the capacitor to charge to near the peak of the input ($V_{p(in)} - 0.7$ V), as shown in Figure 2–63(a). Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near $V_{p(in)} - 0.7$ V by the charge on the capacitor. The capacitor can only discharge through the high resistance of R_L. So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of R_L.

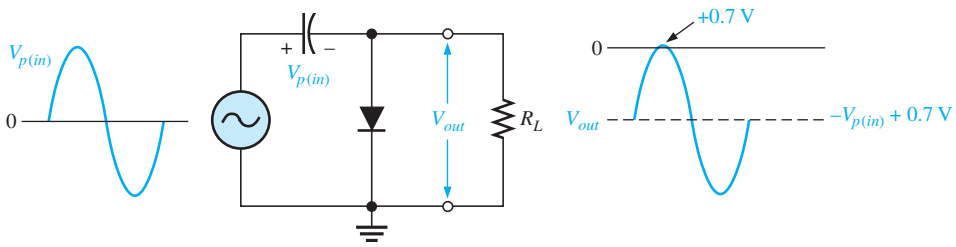


◀ FIGURE 2–63
Positive clamper operation.

If the capacitor discharges during the period of the input wave, clamping action is affected. If the *RC* time constant is 100 times the period, the clamping action is excellent. An *RC* time constant of ten times the period will have a small amount of distortion at the ground level due to the charging current.

The net effect of the clamping action is that the capacitor retains a charge approximately equal to the peak value of the input less the diode drop. The capacitor voltage acts essentially as a battery in series with the input voltage. The dc voltage of the capacitor adds to the input voltage by superposition, as in Figure 2–63(b).

If the diode is turned around, a negative dc voltage is added to the input voltage to produce the output voltage as shown in Figure 2–64.

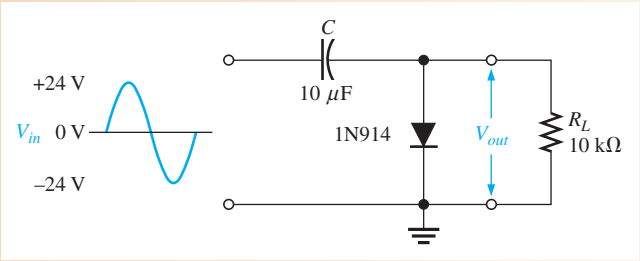


◀ FIGURE 2–64
Negative clamper.

EXAMPLE 2–13

What is the output voltage that you would expect to observe across R_L in the clamping circuit of Figure 2–65? Assume that RC is large enough to prevent significant capacitor discharge.

▶ **FIGURE 2–65**



Solution

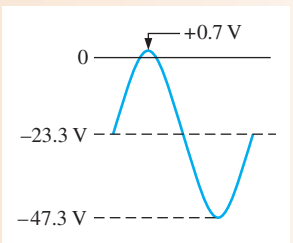
Ideally, a negative dc value equal to the input peak less the diode drop is inserted by the clamping circuit.

$$V_{DC} \cong -(V_{p(in)} - 0.7\text{ V}) = -(24\text{ V} - 0.7\text{ V}) = \mathbf{-23.3\text{ V}}$$

Actually, the capacitor will discharge slightly between peaks, and, as a result, the output voltage will have an average value of slightly less than that calculated above. The output waveform goes to approximately +0.7 V, as shown in Figure 2–66.

▶ **FIGURE 2–66**

Output waveform across R_L for Figure 2–65.



Related Problem

What is the output voltage that you would observe across R_L in Figure 2–65 for $C = 22\ \mu\text{F}$ and $R_L = 18\ \text{k}\Omega$?

Open the Multisim file E02-13 in the Examples folder on the companion website. For the specified input, measure the output waveform. Compare with the waveform shown in the example.

SECTION 2–7 CHECKUP

1. Discuss how diode limiters and diode clampers differ in terms of their function.
2. What is the difference between a positive limiter and a negative limiter?
3. What is the maximum voltage across an unbiased positive silicon diode limiter during the positive alternation of the input voltage?
4. To limit the output voltage of a positive limiter to 5 V when a 10 V peak input is applied, what value must the bias voltage be?
5. What component in a clamping circuit effectively acts as a battery?