

Combinational Logic Analysis

CHAPTER OUTLINE

- 5-1 Basic Combinational Logic Circuits
- 5-2 Implementing Combinational Logic
- 5-3 The Universal Property of NAND and NOR Gates
- 5-4 Combinational Logic Using NAND and NOR Gates
- 5-5 Pulse Waveform Operation
- 5-6 Combinational Logic with VHDL
- 5-7 Troubleshooting Applied Logic

CHAPTER OBJECTIVES

- Analyze basic combinational logic circuits, such as AND-OR, AND-OR-Invert, exclusive-OR, and exclusive-NOR
- Use AND-OR and AND-OR-Invert circuits to implement sum-of-products (SOP) and product-of-sums (POS) expressions
- Write the Boolean output expression for any combinational logic circuit
- Develop a truth table from the output expression for a combinational logic circuit
- Use the Karnaugh map to expand an output expression containing terms with missing variables into a full SOP form
- Design a combinational logic circuit for a given Boolean output expression
- Design a combinational logic circuit for a given truth table
- Simplify a combinational logic circuit to its minimum form
- Use NAND gates to implement any combinational logic function

- Use NOR gates to implement any combinational logic function
- Analyze the operation of logic circuits with pulse inputs
- Write VHDL programs for simple logic circuits
- Troubleshoot faulty logic circuits
- Troubleshoot logic circuits by using signal tracing and waveform analysis
- Apply combinational logic to an application

KEY TERMS

Key terms are in order of appearance in the chapter.

- Universal gate
- Negative-OR
- Negative-AND
- Component
- Signal
- Node
- Signal tracing

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INTRODUCTION

In Chapters 3 and 4, logic gates were discussed on an individual basis and in simple combinations. You were introduced to SOP and POS implementations, which are basic forms of combinational logic. When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is in the category of **combinational logic**. In combinational logic, the output level is at all times dependent on the combination of input levels. This chapter expands on the material introduced in earlier chapters with a coverage of the analysis, design, and troubleshooting of various combinational logic circuits. The VHDL structural approach is introduced and applied to combinational logic.

5-1 Basic Combinational Logic Circuits

In Chapter 4, you learned that SOP expressions are implemented with an AND gate for each product term and one OR gate for summing all of the product terms. As you know, this SOP implementation is called AND-OR logic and is the basic form for realizing standard Boolean functions. In this section, the AND-OR and the AND-OR-Invert are examined; the exclusive-OR and exclusive-NOR gates, which are actually a form of AND-OR logic, are also covered.

After completing this section, you should be able to

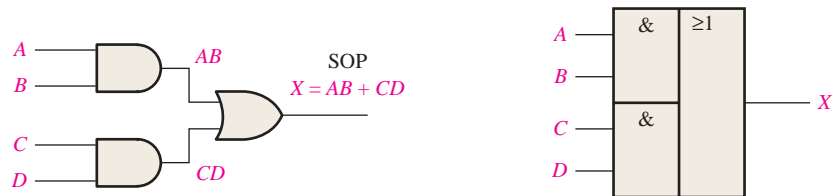
- ◆ Analyze and apply AND-OR circuits
- ◆ Analyze and apply AND-OR-Invert circuits
- ◆ Analyze and apply exclusive-OR gates
- ◆ Analyze and apply exclusive-NOR gates

AND-OR Logic

AND-OR logic produces an SOP expression.

Figure 5-1(a) shows an AND-OR circuit consisting of two 2-input AND gates and one 2-input OR gate; Figure 5-1(b) is the ANSI standard rectangular outline symbol. The Boolean expressions for the AND gate outputs and the resulting SOP expression for the output X are shown on the diagram. In general, an AND-OR circuit can have any number of AND gates, each with any number of inputs.

The truth table for a 4-input AND-OR logic circuit is shown in Table 5-1. The intermediate AND gate outputs (the AB and CD columns) are also shown in the table.



(a) Logic diagram (ANSI standard distinctive shape symbols)

(b) ANSI standard rectangular outline symbol



FIGURE 5-1 An example of AND-OR logic. Open file F05-01 to verify the operation. A Multisim tutorial is available on the website.

TABLE 5-1

Truth table for the AND-OR logic in Figure 5-1.

Inputs				AB	CD	Output X
A	B	C	D			
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	1
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	0	0
0	1	1	1	0	1	1
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

An AND-OR circuit directly implements an SOP expression, assuming the complements (if any) of the variables are available. The operation of the AND-OR circuit in Figure 5-1 is stated as follows:

For a 4-input AND-OR logic circuit, the output X is HIGH (1) if both input A and input B are HIGH (1) or both input C and input D are HIGH (1).

EXAMPLE 5-1

In a certain chemical-processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point.

Design a circuit that monitors the chemical level in each tank and indicates when the level in any two of the tanks drops below the specified point.

Solution

The AND-OR circuit in Figure 5-2 has inputs from the sensors on tanks A , B , and C as shown. The AND gate G_1 checks the levels in tanks A and B , gate G_2 checks tanks A and C , and gate G_3 checks tanks B and C . When the chemical level in any two of the tanks gets too low, one of the AND gates will have HIGHS on both of its inputs, causing its output to be HIGH; and so the final output X from the OR gate is HIGH. This HIGH input is then used to activate an indicator such as a lamp or audible alarm, as shown in the figure.

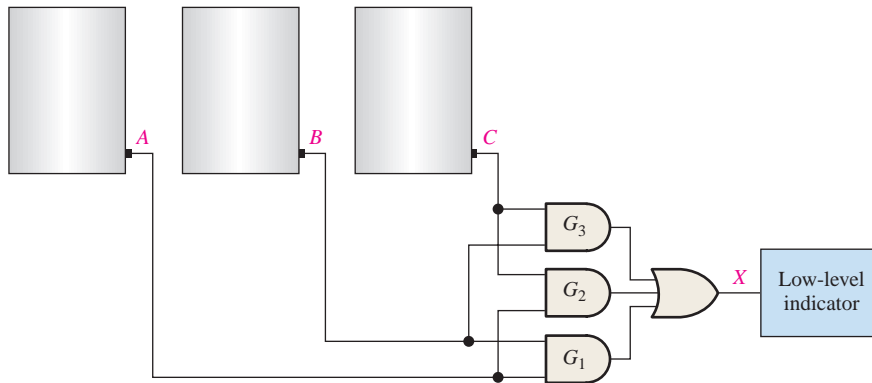


FIGURE 5-2

Related Problem*

Write the Boolean SOP expression for the AND-OR logic in Figure 5-2.

*Answers are at the end of the chapter.

AND-OR-Invert Logic

When the output of an AND-OR circuit is complemented (inverted), it results in an AND-OR-Invert circuit. Recall that AND-OR logic directly implements SOP expressions. POS expressions can be implemented with AND-OR-Invert logic. This is illustrated as follows, starting with a POS expression and developing the corresponding AND-OR-Invert (AOI) expression.

$$X = (\bar{A} + \bar{B})(\bar{C} + \bar{D}) = \overline{(\overline{\bar{A} + \bar{B}})(\overline{\bar{C} + \bar{D}})} = \overline{(\overline{AB})(\overline{CD})} = \overline{AB} + \overline{CD} = \overline{AB} + \overline{CD}$$

The logic diagram in Figure 5-3(a) shows an AND-OR-Invert circuit with four inputs and the development of the POS output expression. The ANSI standard rectangular outline symbol is shown in part (b). In general, an AND-OR-Invert circuit can have any number of AND gates, each with any number of inputs.

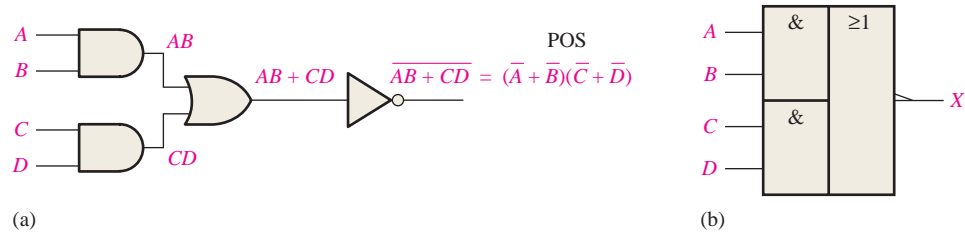


FIGURE 5-3 An AND-OR-Invert circuit produces a POS output. Open file F05-03 to verify the operation.

The operation of the AND-OR-Invert circuit in Figure 5-3 is stated as follows:

For a 4-input AND-OR-Invert logic circuit, the output X is LOW (0) if both input A and input B are HIGH (1) or both input C and input D are HIGH (1).

A truth table can be developed from the AND-OR truth table in Table 5-1 by simply changing all 1s to 0s and all 0s to 1s in the output column.

EXAMPLE 5-2

The sensors in the chemical tanks of Example 5-1 are being replaced by a new model that produces a LOW voltage instead of a HIGH voltage when the level of the chemical in the tank drops below a critical point.

Modify the circuit in Figure 5-2 to operate with the different input levels and still produce a HIGH output to activate the indicator when the level in any two of the tanks drops below the critical point. Show the logic diagram.

Solution

The AND-OR-Invert circuit in Figure 5-4 has inputs from the sensors on tanks A , B , and C as shown. The AND gate G_1 checks the levels in tanks A and B , gate G_2 checks tanks A and C , and gate G_3 checks tanks B and C . When the chemical level in any two of the tanks gets too low, each AND gate will have a LOW on at least one input, causing its output to be LOW and, thus, the final output X from the inverter is HIGH. This HIGH output is then used to activate an indicator.

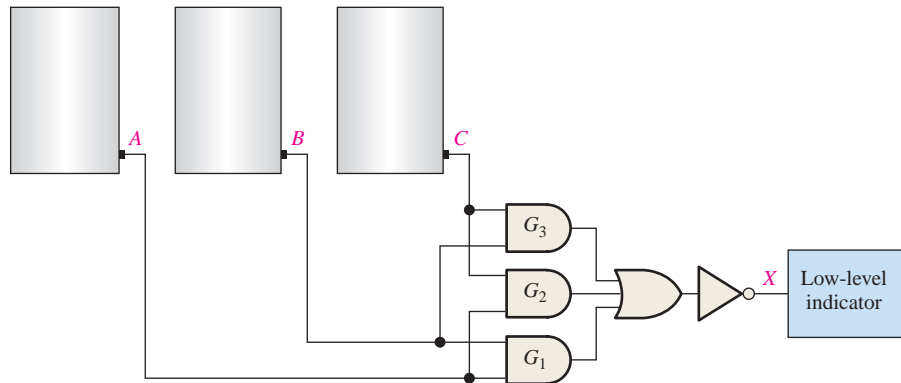


FIGURE 5-4

Related Problem

Write the Boolean expression for the AND-OR-Invert logic in Figure 5-4 and show that the output is HIGH (1) when any two of the inputs A , B , and C are LOW (0).

Exclusive-OR Logic

The exclusive-OR gate was introduced in Chapter 3. Although this circuit is considered a type of logic gate with its own unique symbol, it is actually a combination of two AND gates, one OR gate, and two inverters, as shown in Figure 5–5(a). The two ANSI standard exclusive-OR logic symbols are shown in parts (b) and (c).

The XOR gate is actually a combination of other gates.

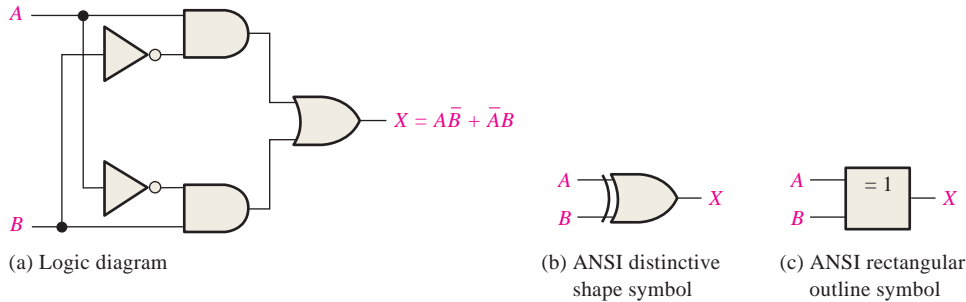


FIGURE 5-5 Exclusive-OR logic diagram and symbols. Open file F05-05 to verify the operation.



The output expression for the circuit in Figure 5–5 is

$$X = A\bar{B} + \bar{A}B$$

Evaluation of this expression results in the truth table in Table 5–2. Notice that the output is HIGH only when the two inputs are at opposite levels. A special exclusive-OR operator \oplus is often used, so the expression $X = A\bar{B} + \bar{A}B$ can be stated as “X is equal to A exclusive-OR B” and can be written as

$$X = A \oplus B$$

TABLE 5-2

Truth table for an exclusive-OR.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-NOR Logic

As you know, the complement of the exclusive-OR function is the exclusive-NOR, which is derived as follows:

$$X = \overline{A\bar{B} + \bar{A}B} = \overline{(A\bar{B})} \overline{(\bar{A}B)} = (\bar{A} + B)(A + \bar{B}) = \bar{A}\bar{B} + AB$$

Notice that the output X is HIGH only when the two inputs, A and B, are at the same level.

The exclusive-NOR can be implemented by simply inverting the output of an exclusive-OR, as shown in Figure 5–6(a), or by directly implementing the expression $\bar{A}\bar{B} + AB$, as shown in part (b).

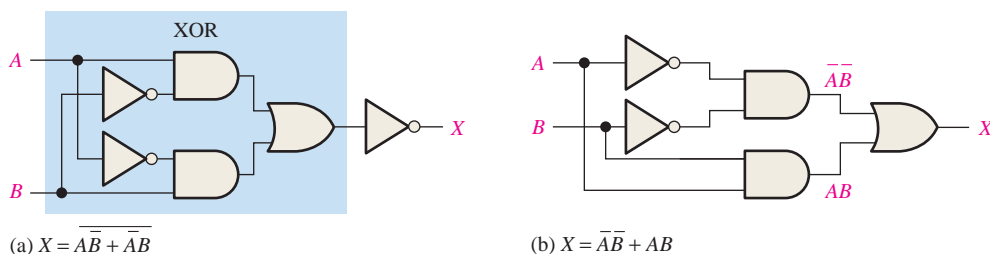


FIGURE 5-6 Two equivalent ways of implementing the exclusive-NOR. Open files F05-06 (a) and (b) to verify the operation.



EXAMPLE 5-3

Use exclusive-OR gates to implement an even-parity code generator for an original 4-bit code.

Solution

Recall from Chapter 2 that a parity bit is added to a binary code in order to provide error detection. For even parity, a parity bit is added to the original code to make the total number of 1s in the code even. The circuit in Figure 5-7 produces a 1 output when there is an odd number of 1s on the inputs in order to make the total number of 1s in the output code even. A 0 output is produced when there is an even number of 1s on the inputs.

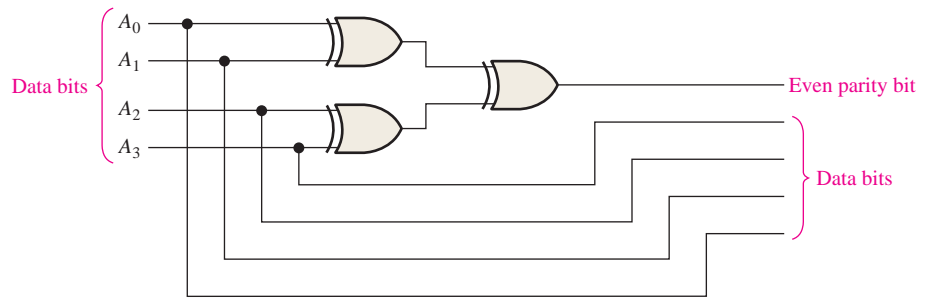


FIGURE 5-7 Even-parity generator.

Related Problem

How would you verify that a correct even-parity bit is generated for each combination of the four data bits?

EXAMPLE 5-4

Use exclusive-OR gates to implement an even-parity checker for the 5-bit code generated by the circuit in Example 5-3.

Solution

The circuit in Figure 5-8 produces a 1 output when there is an error in the five-bit code and a 0 when there is no error.

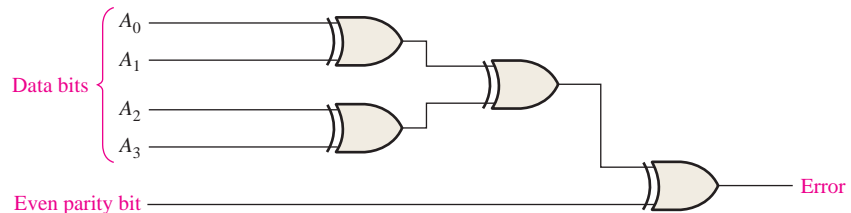


FIGURE 5-8 Even-parity checker.

Related Problem

How would you verify that an error is indicated when the input code is incorrect?

SECTION 5-1 CHECKUP

Answers are at the end of the chapter.

- Determine the output (1 or 0) of a 4-variable AND-OR-Invert circuit for each of the following input conditions:
 - $A = 1, B = 0, C = 1, D = 0$
 - $A = 1, B = 1, C = 0, D = 1$
 - $A = 0, B = 1, C = 1, D = 1$
- Determine the output (1 or 0) of an exclusive-OR gate for each of the following input conditions:
 - $A = 1, B = 0$
 - $A = 1, B = 1$
 - $A = 0, B = 1$
 - $A = 0, B = 0$
- Develop the truth table for a certain 3-input logic circuit with the output expression $X = \overline{A}BC + A\overline{B}C + A\overline{B}\overline{C} + ABC + ABC$.
- Draw the logic diagram for an exclusive-NOR circuit.

5-2 Implementing Combinational Logic

In this section, examples are used to illustrate how to implement a logic circuit from a Boolean expression or a truth table. Minimization of a logic circuit using the methods covered in Chapter 4 is also included.

After completing this section, you should be able to

- ◆ Implement a logic circuit from a Boolean expression
- ◆ Implement a logic circuit from a truth table
- ◆ Minimize a logic circuit

For every Boolean expression there is a logic circuit, and for every logic circuit there is a Boolean expression.

From a Boolean Expression to a Logic Circuit

Let's examine the following Boolean expression:

$$X = AB + CDE$$

A brief inspection shows that this expression is composed of two terms, AB and CDE , with a domain of five variables. The first term is formed by ANDing A with B , and the second term is formed by ANDing C , D , and E . The two terms are then ORed to form the output X . These operations are indicated in the structure of the expression as follows:

$$X = \overline{\overline{AB}} + \overline{\overline{CDE}}$$

Note that in this particular expression, the AND operations forming the two individual terms, AB and CDE , must be performed *before* the terms can be ORed.

To implement this Boolean expression, a 2-input AND gate is required to form the term AB , and a 3-input AND gate is needed to form the term CDE . A 2-input OR gate is then required to combine the two AND terms. The resulting logic circuit is shown in Figure 5-9.

As another example, let's implement the following expression:

$$X = AB(\overline{C}\overline{D} + EF)$$

InfoNote

Many control programs require logic operations to be performed by a computer. A driver program is a control program that is used with computer peripherals. For example, a mouse driver requires logic tests to determine if a button has been pressed and further logic operations to determine if it has moved, either horizontally or vertically. Within the heart of a microprocessor is the arithmetic logic unit (ALU), which performs these logic operations as directed by program instructions. All of the logic described in this chapter can also be performed by the ALU, given the proper instructions.

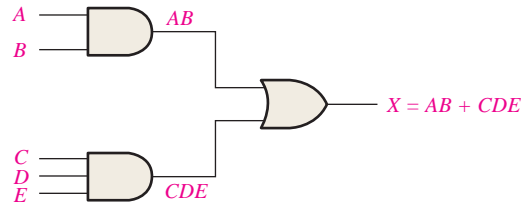
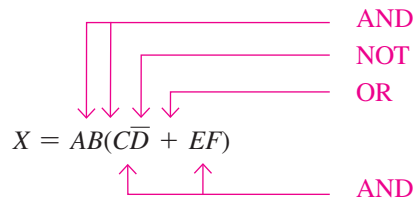


FIGURE 5-9 Logic circuit for $X = AB + CDE$.

A breakdown of this expression shows that the terms AB and $(\overline{C}\overline{D} + EF)$ are ANDed. The term $\overline{C}\overline{D} + EF$ is formed by first ANDing C and \overline{D} and ANDing E and F , and then ORing these two terms. This structure is indicated in relation to the expression as follows:



Before you can implement the final expression, you must create the sum term $\overline{C}\overline{D} + EF$; but before you can get this term; you must create the product terms $\overline{C}\overline{D}$ and EF ; but before you can get the term $\overline{C}\overline{D}$, you must create \overline{D} . So, as you can see, the logic operations must be done in the proper order.

The logic gates required to implement $X = AB(\overline{C}\overline{D} + EF)$ are as follows:

1. One inverter to form \overline{D}
2. Two 2-input AND gates to form $\overline{C}\overline{D}$ and EF
3. One 2-input OR gate to form $\overline{C}\overline{D} + EF$
4. One 3-input AND gate to form X

The logic circuit for this expression is shown in Figure 5-10(a). Notice that there is a maximum of four gates and an inverter between an input and output in this circuit (from input D to output). Often the total propagation delay time through a logic circuit is a major consideration. Propagation delays are additive, so the more gates or inverters between input and output, the greater the propagation delay time.

Unless an intermediate term, such as $\overline{C}\overline{D} + EF$ in Figure 5-10(a), is required as an output for some other purpose, it is usually best to reduce a circuit to its SOP form in order to reduce the overall propagation delay time. The expression is converted to SOP as follows, and the resulting circuit is shown in Figure 5-10(b).

$$AB(\overline{C}\overline{D} + EF) = ABC\overline{D} + ABEF$$

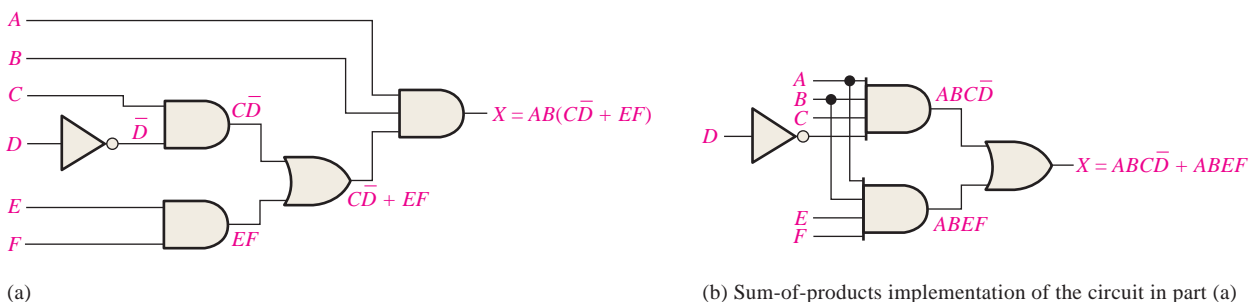


FIGURE 5-10 Logic circuits for $X = AB(\overline{C}\overline{D} + EF) = ABC\overline{D} + ABEF$.

TABLE 5-3				
Inputs			Output	Product Term
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	1	$A\overline{B}\overline{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

From a Truth Table to a Logic Circuit

If you begin with a truth table instead of an expression, you can write the SOP expression from the truth table and then implement the logic circuit. Table 5-3 specifies a logic function.

The Boolean SOP expression obtained from the truth table by ORing the product terms for which $X = 1$ is

$$X = \overline{A}BC + A\overline{B}\overline{C}$$

The first term in the expression is formed by ANDing the three variables \overline{A} , B , and C . The second term is formed by ANDing the three variables A , \overline{B} , and \overline{C} .

The logic gates required to implement this expression are as follows: three inverters to form the \overline{A} , \overline{B} , and \overline{C} variables; two 3-input AND gates to form the terms $\overline{A}BC$ and $A\overline{B}\overline{C}$; and one 2-input OR gate to form the final output function, $\overline{A}BC + A\overline{B}\overline{C}$.

The implementation of this logic function is illustrated in Figure 5-11.

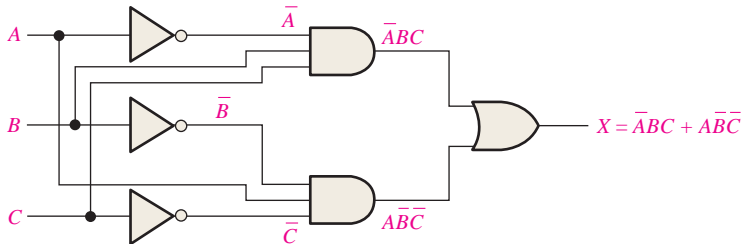


FIGURE 5-11 Logic circuit for $X = \overline{A}BC + A\overline{B}\overline{C}$. Open file F05-11 to verify the operation.



EXAMPLE 5-5

Design a logic circuit to implement the operation specified in the truth table of Table 5-4.

TABLE 5-4				
Inputs			Output	Product Term
A	B	C	X	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\overline{A}BC$
1	0	0	0	
1	0	1	1	$A\overline{B}C$
1	1	0	1	$AB\overline{C}$
1	1	1	0	

Solution

Notice that $X = 1$ for only three of the input conditions. Therefore, the logic expression is

$$X = \overline{A}BC + A\overline{B}C + AB\overline{C}$$

The logic gates required are three inverters, three 3-input AND gates and one 3-input OR gate. The logic circuit is shown in Figure 5–12.

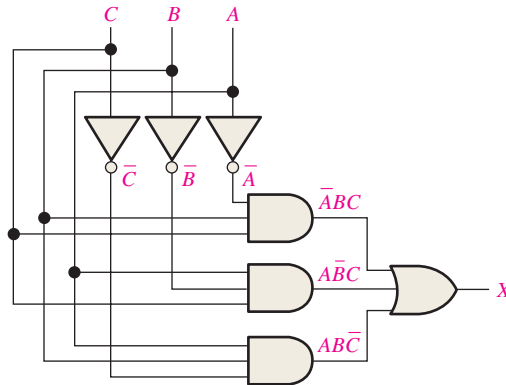


FIGURE 5-12 Open file F05-12 to verify the operation.

MultiSim

Related Problem

Determine if the logic circuit of Figure 5–12 can be simplified.

EXAMPLE 5-6

Develop a logic circuit with four input variables that will only produce a 1 output when exactly three input variables are 1s.

Solution

Out of sixteen possible combinations of four variables, the combinations in which there are exactly three 1s are listed in Table 5–5, along with the corresponding product term for each.

TABLE 5-5

A	B	C	D	Product Term
0	1	1	1	$\bar{A}BCD$
1	0	1	1	$A\bar{B}CD$
1	1	0	1	$AB\bar{C}D$
1	1	1	0	$ABC\bar{D}$

The product terms are ORed to get the following expression:

$$X = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$$

This expression is implemented in Figure 5–13 with AND-OR logic.

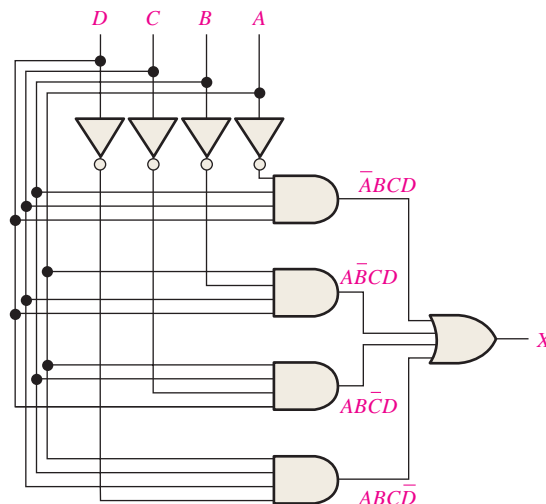


FIGURE 5-13 Open file F05-13 to verify the operation.

MultiSim

Related Problem

Determine if the logic circuit of Figure 5–13 can be simplified.

EXAMPLE 5-7

Reduce the combinational logic circuit in Figure 5–14 to a minimum form.

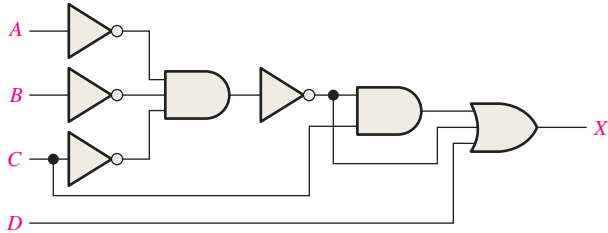


FIGURE 5-14
Open file F05-14 to verify that this circuit is equivalent to the gate in Figure 5–15.



Solution

The expression for the output of the circuit is

$$X = (\overline{\overline{A}\overline{B}\overline{C}})C + \overline{\overline{A}\overline{B}\overline{C}} + D$$

Applying DeMorgan’s theorem and Boolean algebra,

$$\begin{aligned} X &= (\overline{\overline{A} + \overline{B} + \overline{C}})C + \overline{\overline{A} + \overline{B} + \overline{C}} + D \\ &= AC + BC + CC + A + B + C + D \\ &= AC + BC + C + A + B + C + D \\ &= C(A + B + 1) + A + B + D \\ X &= A + B + C + D \end{aligned}$$

The simplified circuit is a 4-input OR gate as shown in Figure 5–15.

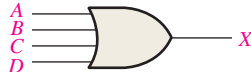


FIGURE 5-15

Related Problem

Verify the minimized expression $A + B + C + D$ using a Karnaugh map.

EXAMPLE 5-8

Minimize the combinational logic circuit in Figure 5–16. Inverters for the complemented variables are not shown.

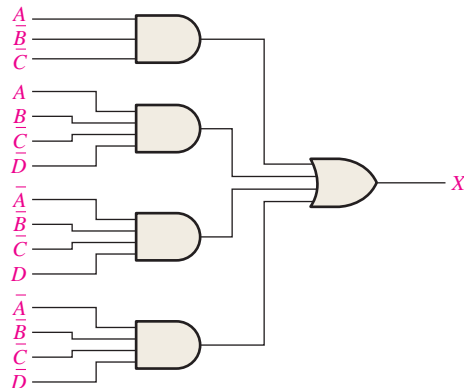


FIGURE 5-16

Solution

The output expression is

$$X = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}C\overline{D}$$

Expanding the first term to include the missing variables D and \overline{D} ,

$$\begin{aligned} X &= \overline{A}\overline{B}\overline{C}(D + \overline{D}) + \overline{A}B\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}C\overline{D} \\ &= \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}C\overline{D} \end{aligned}$$

This expanded SOP expression is mapped and simplified on the Karnaugh map in Figure 5–17(a). The simplified implementation is shown in part (b). Inverters are not shown.

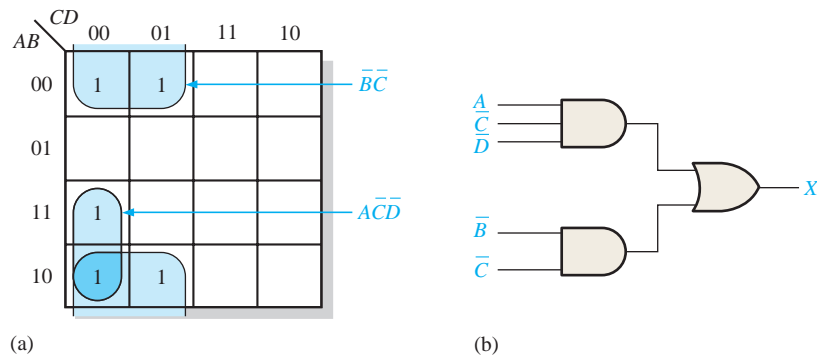


FIGURE 5–17

Related Problem

Develop the POS equivalent of the circuit in Figure 5–17(b). See Section 4–10.

SECTION 5–2 CHECKUP

1. Implement the following Boolean expressions as they are stated:

(a) $X = ABC + AB + AC$ (b) $X = AB(C + DE)$

2. Develop a logic circuit that will produce a 1 on its output only when all three inputs are 1s or when all three inputs are 0s.

3. Reduce the circuits in Question 1 to minimum SOP form.

5–3 The Universal Property of NAND and NOR Gates

Up to this point, you have studied combinational circuits implemented with AND gates, OR gates, and inverters. In this section, the universal property of the NAND gate and the NOR gate is discussed. The universality of the NAND gate means that it can be used as an inverter and that combinations of NAND gates can be used to implement the AND, OR, and NOR operations. Similarly, the NOR gate can be used to implement the inverter (NOT), AND, OR, and NAND operations.

After completing this section, you should be able to

- ♦ Use NAND gates to implement the inverter, the AND gate, the OR gate, and the NOR gate
- ♦ Use NOR gates to implement the inverter, the AND gate, the OR gate, and the NAND gate

The NAND Gate as a Universal Logic Element

The NAND gate is a **universal gate** because it can be used to produce the NOT, the AND, the OR, and the NOR functions. An inverter can be made from a NAND gate by connecting all of the inputs together and creating, in effect, a single input, as shown in Figure 5–18(a) for a 2-input gate. An AND function can be generated by the use of NAND gates alone, as shown in Figure 5–18(b). An OR function can be produced with only NAND gates, as illustrated in part (c). Finally, a NOR function is produced as shown in part (d).

Combinations of NAND gates can be used to produce any logic function.

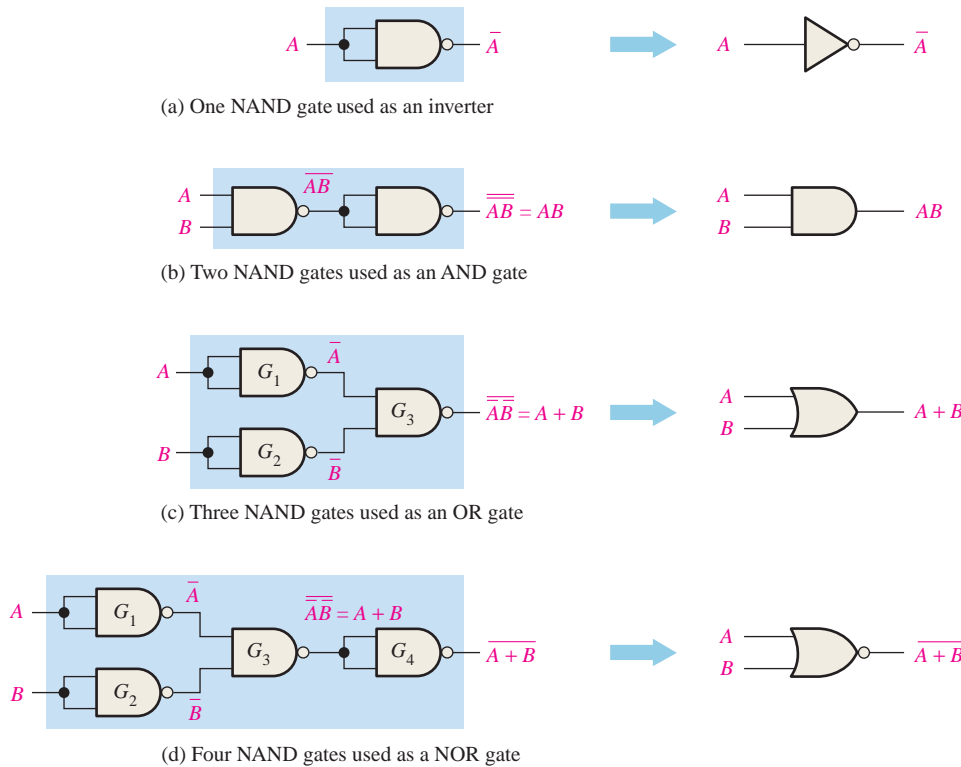


FIGURE 5-18 Universal application of NAND gates. Open files F05-18(a), (b), (c), and (d) to verify each of the equivalencies.



In Figure 5–18(b), a NAND gate is used to invert (complement) a NAND output to form the AND function, as indicated in the following equation:

$$X = \overline{\overline{AB}} = AB$$

In Figure 5–18(c), NAND gates G_1 and G_2 are used to invert the two input variables before they are applied to NAND gate G_3 . The final OR output is derived as follows by application of DeMorgan's theorem:

$$X = \overline{\overline{A} \overline{B}} = A + B$$

In Figure 5–18(d), NAND gate G_4 is used as an inverter connected to the circuit of part (c) to produce the NOR operation $\overline{A + B}$.

The NOR Gate as a Universal Logic Element

Like the NAND gate, the NOR gate can be used to produce the NOT, AND, OR, and NAND functions. A NOT circuit, or inverter, can be made from a NOR gate by connecting all of the inputs together to effectively create a single input, as shown in Figure 5–19(a) with a 2-input example. Also, an OR gate can be produced from NOR gates, as illustrated in Figure 5–19(b). An AND gate can be constructed by the use of NOR gates, as shown in

Combinations of NOR gates can be used to produce any logic function.

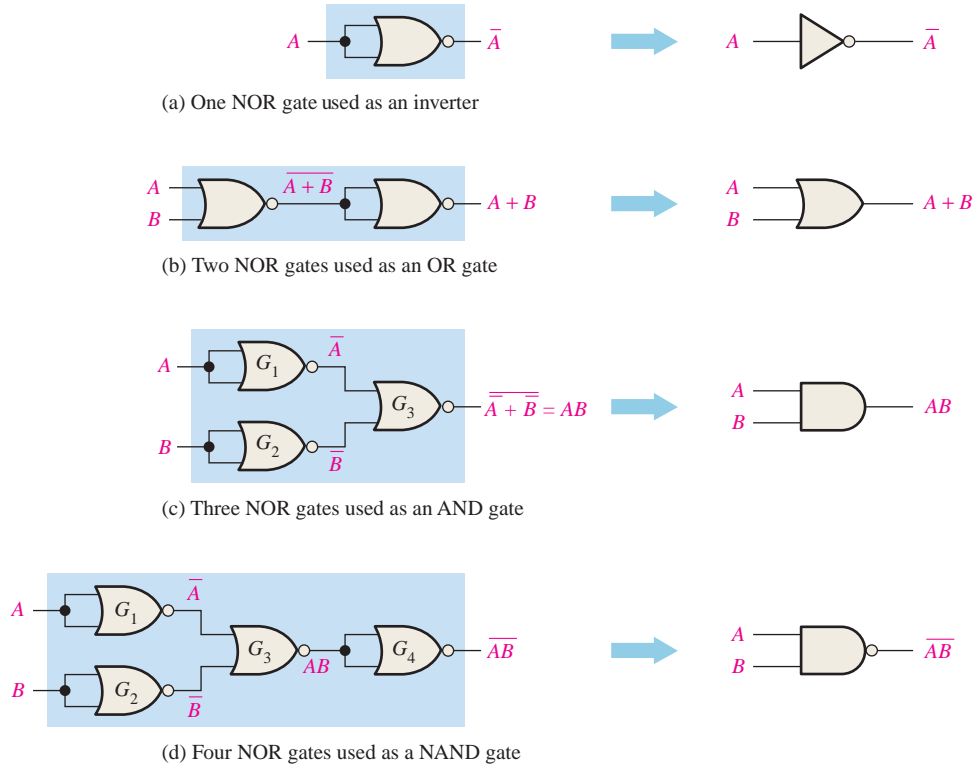


FIGURE 5-19 Universal application of NOR gates. Open files F05-19(a), (b), (c), and (d) to verify each of the equivalencies.

Figure 5–19(c). In this case the NOR gates G_1 and G_2 are used as inverters, and the final output is derived by the use of DeMorgan’s theorem as follows:

$$X = \overline{\overline{A} + \overline{B}} = AB$$

Figure 5–19(d) shows how NOR gates are used to form a NAND function.

SECTION 5-3 CHECKUP

1. Use NAND gates to implement each expression:
 - (a) $X = \overline{A} + B$
 - (b) $X = A\overline{B}$
2. Use NOR gates to implement each expression:
 - (a) $X = \overline{A} + B$
 - (b) $X = A\overline{B}$

5-4 Combinational Logic Using NAND and NOR Gates

In this section, you will see how NAND and NOR gates can be used to implement a logic function. Recall from Chapter 3 that the NAND gate also exhibits an equivalent operation called the negative-OR and that the NOR gate exhibits an equivalent operation called the negative-AND. You will see how the use of the appropriate symbols to represent the equivalent operations makes “reading” a logic diagram easier.

After completing this section, you should be able to

- ♦ Use NAND gates to implement a logic function
- ♦ Use NOR gates to implement a logic function
- ♦ Use the appropriate dual symbol in a logic diagram

NAND Logic

As you have learned, a NAND gate can function as either a NAND or a negative-OR because, by DeMorgan's theorem,

$$\overline{AB} = \overline{A} + \overline{B}$$

NAND
negative-OR

Consider the NAND logic in Figure 5-20. The output expression is developed in the following steps:

$$\begin{aligned} X &= \overline{(\overline{AB})(\overline{CD})} \\ &= \overline{(\overline{A} + \overline{B})(\overline{C} + \overline{D})} \\ &= \overline{(\overline{A} + \overline{B})} + \overline{(\overline{C} + \overline{D})} \\ &= \overline{\overline{A}}\overline{\overline{B}} + \overline{\overline{C}}\overline{\overline{D}} \\ &= AB + CD \end{aligned}$$

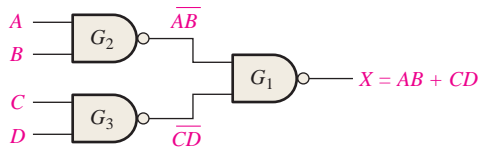
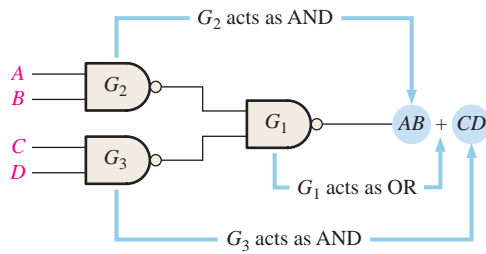


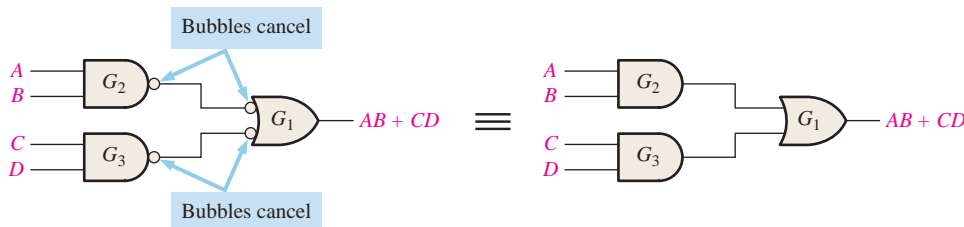
FIGURE 5-20 NAND logic for $X = AB + CD$.

As you can see in Figure 5-20, the output expression, $AB + CD$, is in the form of two AND terms ORed together. This shows that gates G_2 and G_3 act as AND gates and that gate G_1 acts as an OR gate, as illustrated in Figure 5-21(a). This circuit is redrawn in part (b) with NAND symbols for gates G_2 and G_3 and a negative-OR symbol for gate G_1 .

Notice in Figure 5-21(b) the bubble-to-bubble connections between the outputs of gates G_2 and G_3 and the inputs of gate G_1 . Since a bubble represents an inversion, two



(a) Original NAND logic diagram showing effective gate operation relative to the output expression



(b) Equivalent NAND/Negative-OR logic diagram

(c) AND-OR equivalent

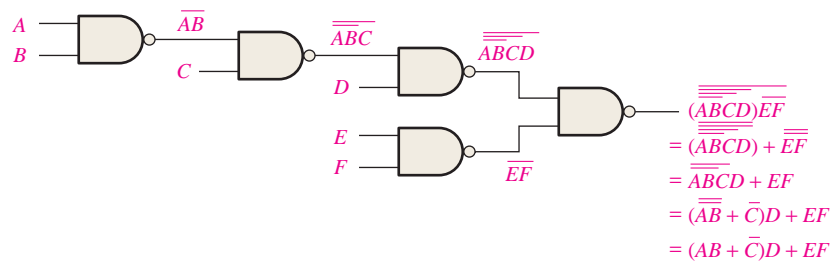
FIGURE 5-21 Development of the AND-OR equivalent of the circuit in Figure 5-20.

connected bubbles represent a double inversion and therefore cancel each other. This inversion cancellation can be seen in the previous development of the output expression $AB + CD$ and is indicated by the absence of barred terms in the output expression. Thus, the circuit in Figure 5–21(b) is effectively an AND-OR circuit, as shown in Figure 5–21(c).

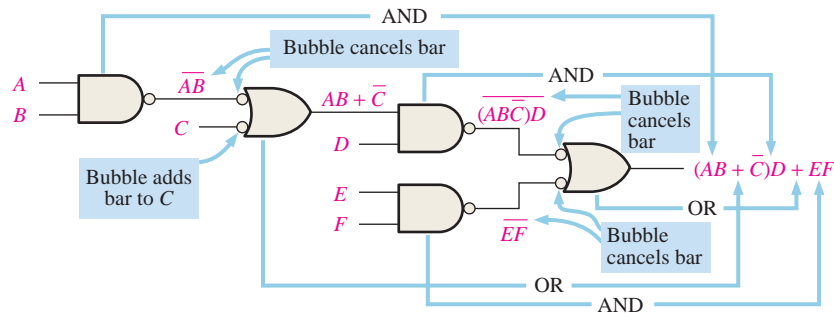
NAND Logic Diagrams Using Dual Symbols

All logic diagrams using NAND gates should be drawn with each gate represented by either a NAND symbol or the equivalent negative-OR symbol to reflect the operation of the gate within the logic circuit. The NAND symbol and the **negative-OR** symbol are called *dual symbols*. When drawing a NAND logic diagram, always use the gate symbols in such a way that every connection between a gate output and a gate input is either bubble-to-bubble or nonbubble-to-nonbubble. In general, a bubble output should not be connected to a nonbubble input or vice versa in a logic diagram.

Figure 5–22 shows an arrangement of gates to illustrate the procedure of using the appropriate dual symbols for a NAND circuit with several gate levels. Although using all NAND symbols as in Figure 5–22(a) is correct, the diagram in part (b) is much easier to “read” and is the preferred method. As shown in Figure 5–22(b), the output gate is represented with a negative-OR symbol. Then the NAND symbol is used for the level of gates right before the output gate and the symbols for successive levels of gates are alternated as you move away from the output.



(a) Several Boolean steps are required to arrive at final output expression.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

FIGURE 5–22 Illustration of the use of the appropriate dual symbols in a NAND logic diagram.

The shape of the gate indicates the way its inputs will appear in the output expression and thus shows how the gate functions within the logic circuit. For a NAND symbol, the inputs appear ANDed in the output expression; and for a negative-OR symbol, the inputs appear ORed in the output expression, as Figure 5–22(b) illustrates. The dual-symbol diagram in part (b) makes it easier to determine the output expression directly from the logic diagram because each gate symbol indicates the relationship of its input variables as they appear in the output expression.

EXAMPLE 5-9

Redraw the logic diagram and develop the output expression for the circuit in Figure 5-23 using the appropriate dual symbols.

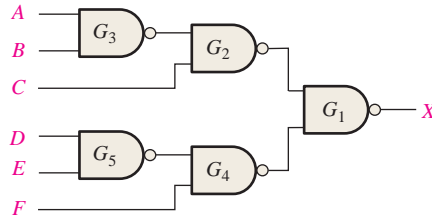


FIGURE 5-23

Solution

Redraw the logic diagram in Figure 5-23 with the use of equivalent negative-OR symbols as shown in Figure 5-24. Writing the expression for X directly from the indicated logic operation of each gate gives $X = (\bar{A} + \bar{B})C + (\bar{D} + \bar{E})F$.

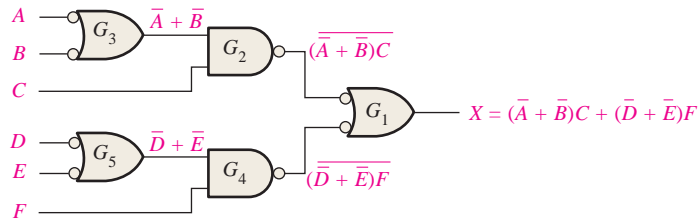


FIGURE 5-24

Related Problem

Derive the output expression from Figure 5-23 and show it is equivalent to the expression in the solution.

EXAMPLE 5-10

Implement each expression with NAND logic using appropriate dual symbols:

- (a) $ABC + DE$
- (b) $ABC + \bar{D} + \bar{E}$

Solution

See Figure 5-25.

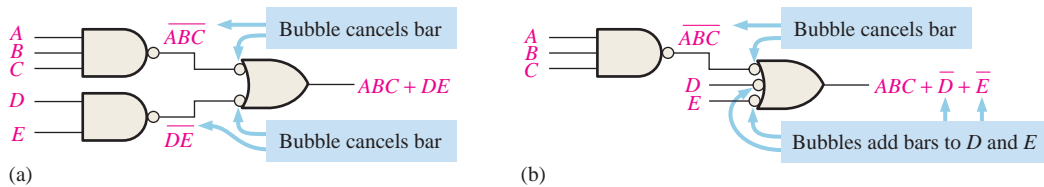


FIGURE 5-25

Related Problem

Convert the NAND circuits in Figure 5-25(a) and (b) to equivalent AND-OR logic.

NOR Logic

A NOR gate can function as either a NOR or a **negative-AND**, as shown by DeMorgan's theorem.

$$\overline{A + B} = \bar{A}\bar{B}$$

↑
↑

NOR
negative-AND

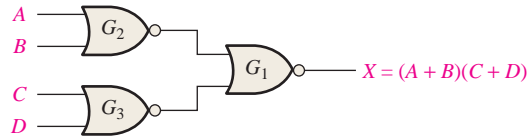


FIGURE 5-26 NOR logic for $X = (A + B)(C + D)$.

Consider the NOR logic in Figure 5-26. The output expression is developed as follows:

$$X = \overline{\overline{A + B + C + D}} = \overline{(\overline{A + B})(\overline{C + D})} = (A + B)C + D$$

As you can see in Figure 5-26, the output expression $(A + B)(C + D)$ consists of two OR terms ANDed together. This shows that gates G_2 and G_3 act as OR gates and gate G_1 acts as an AND gate, as illustrated in Figure 5-27(a). This circuit is redrawn in part (b) with a negative-AND symbol for gate G_1 .

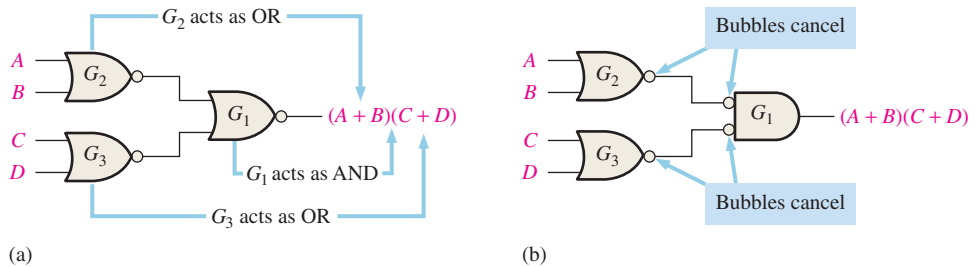
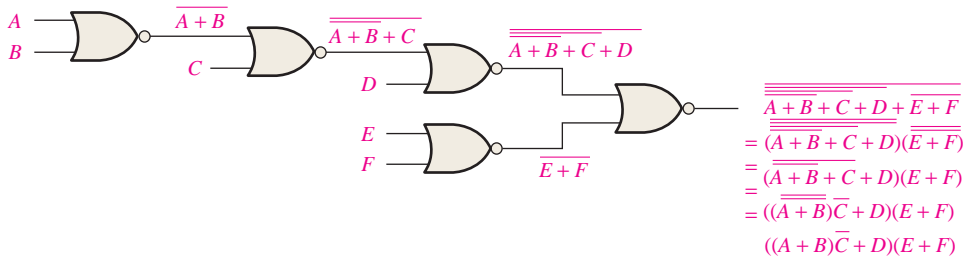


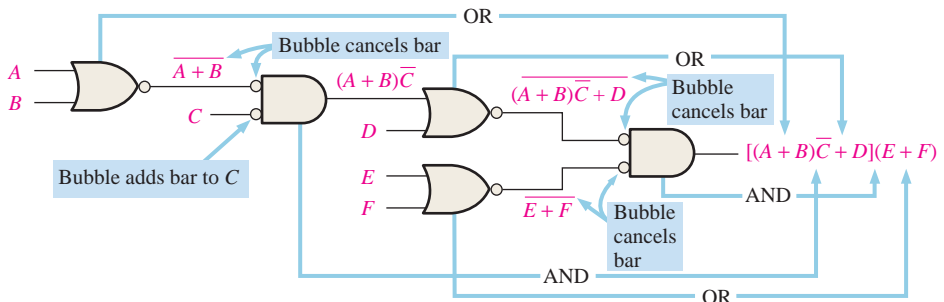
FIGURE 5-27

NOR Logic Diagram Using Dual Symbols

As with NAND logic, the purpose for using the dual symbols is to make the logic diagram easier to read and analyze, as illustrated in the NOR logic circuit in Figure 5-28. When the circuit in part (a) is redrawn with dual symbols in part (b), notice that all output-to-input



(a) Final output expression is obtained after several Boolean steps.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

FIGURE 5-28 Illustration of the use of the appropriate dual symbols in a NOR logic diagram.

connections between gates are bubble-to-bubble or nonbubble-to-nonbubble. Again, you can see that the shape of each gate symbol indicates the type of term (AND or OR) that it produces in the output expression, thus making the output expression easier to determine and the logic diagram easier to analyze.

EXAMPLE 5-11

Using appropriate dual symbols, redraw the logic diagram and develop the output expression for the circuit in Figure 5-29.

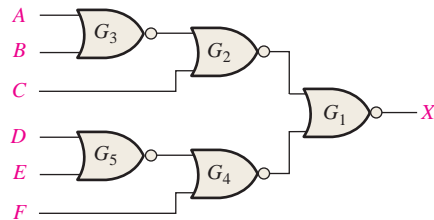


FIGURE 5-29

Solution

Redraw the logic diagram with the equivalent negative-AND symbols as shown in Figure 5-30. Writing the expression for X directly from the indicated operation of each gate,

$$X = (\overline{A\overline{B}} + C)(\overline{\overline{D\overline{E}} + F})$$

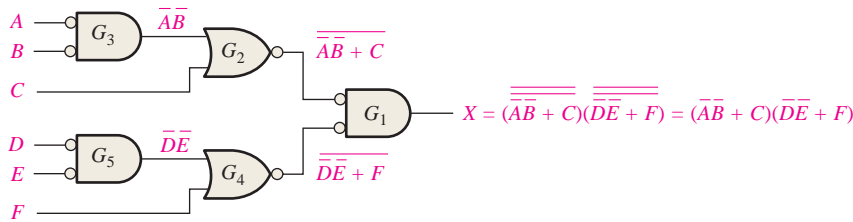


FIGURE 5-30

Related Problem

Prove that the output of the NOR circuit in Figure 5-29 is the same as for the circuit in Figure 5-30.

SECTION 5-4 CHECKUP

1. Implement the expression $X = \overline{(\overline{A} + \overline{B} + \overline{C})DE}$ by using NAND logic.
2. Implement the expression $X = \overline{\overline{A\overline{B\overline{C}}} + (D + E)}$ with NOR logic.

5-5 Pulse Waveform Operation

General combinational logic circuits with pulse waveform inputs are examined in this section. Keep in mind that the operation of each gate is the same for pulse waveform inputs as for constant-level inputs. The output of a logic circuit at any given time depends on the inputs at that particular time, so the relationship of the time-varying inputs is of primary importance.

After completing this section, you should be able to

- ◆ Analyze combinational logic circuits with pulse waveform inputs
- ◆ Develop a timing diagram for any given combinational logic circuit with specified inputs

The operation of any gate is the same regardless of whether its inputs are pulsed or constant levels. The nature of the inputs (pulsed or constant levels) does not alter the truth table of a circuit. The examples in this section illustrate the analysis of combinational logic circuits with pulse waveform inputs.

The following is a review of the operation of individual gates for use in analyzing combinational circuits with pulse waveform inputs:

1. The output of an AND gate is HIGH only when all inputs are HIGH at the same time.
2. The output of an OR gate is HIGH only when at least one of its inputs is HIGH.
3. The output of a NAND gate is LOW only when all inputs are HIGH at the same time.
4. The output of a NOR gate is LOW only when at least one of its inputs is HIGH.

EXAMPLE 5-12

Determine the final output waveform X for the circuit in Figure 5-31, with input waveforms A , B , and C as shown.

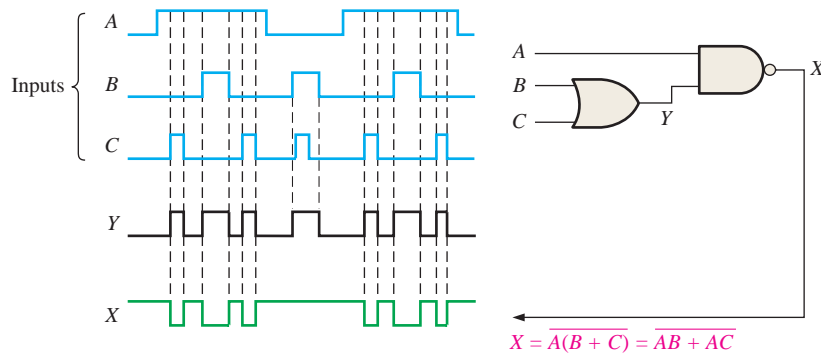


FIGURE 5-31

Solution

The output expression, $\overline{AB + AC}$, indicates that the output X is LOW when both A and B are HIGH or when both A and C are HIGH or when all inputs are HIGH. The output waveform X is shown in the timing diagram of Figure 5-31. The intermediate waveform Y at the output of the OR gate is also shown.

Related Problem

Determine the output waveform if input A is a constant HIGH level.

EXAMPLE 5-13

Draw the timing diagram for the circuit in Figure 5-32 showing the outputs of G_1 , G_2 , and G_3 with the input waveforms, A , and B , as indicated.

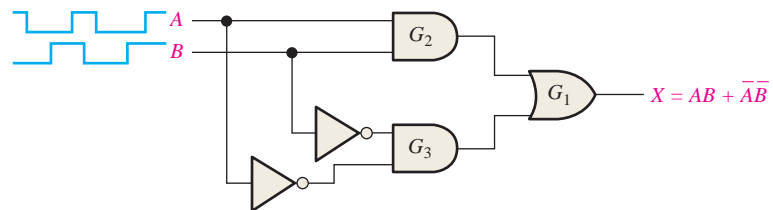
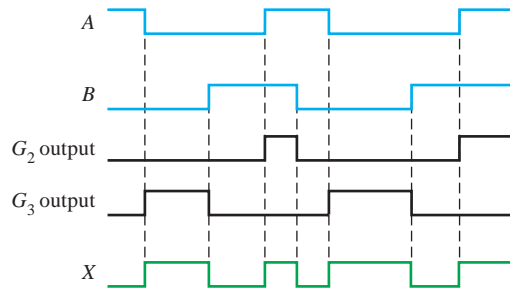


FIGURE 5-32

Solution

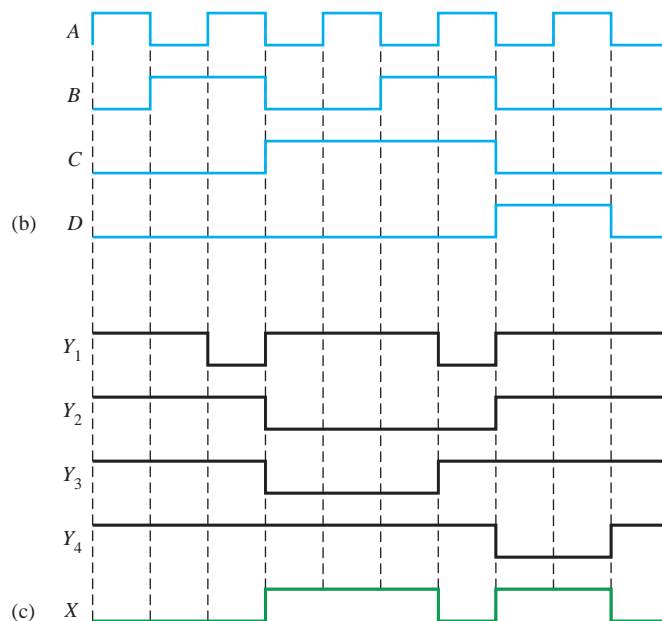
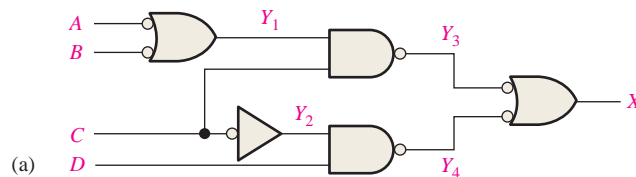
When both inputs are HIGH or when both inputs are LOW, the output X is HIGH as shown in Figure 5–33. Notice that this is an exclusive-NOR circuit. The intermediate outputs of gates G_2 and G_3 are also shown in Figure 5–33.

**FIGURE 5-33****Related Problem**

Determine the output X in Figure 5–32 if input B is inverted.

EXAMPLE 5-14

Determine the output waveform X for the logic circuit in Figure 5–34(a) by first finding the intermediate waveform at each of points Y_1 , Y_2 , Y_3 , and Y_4 . The input waveforms are shown in Figure 5–34(b).

**FIGURE 5-34**

Solution

All the intermediate waveforms and the final output waveform are shown in the timing diagram of Figure 5–34(c).

Related Problem

Determine the waveforms Y_1, Y_2, Y_3, Y_4 and X if input waveform A is inverted.

EXAMPLE 5-15

Determine the output waveform X for the circuit in Example 5–14, Figure 5–34(a), directly from the output expression.

Solution

The output expression for the circuit is developed in Figure 5–35. The SOP form indicates that the output is HIGH when A is LOW and C is HIGH or when B is LOW and C is HIGH or when C is LOW and D is HIGH.

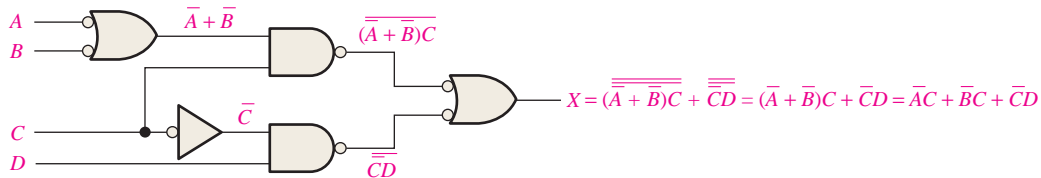


FIGURE 5-35

The result is shown in Figure 5–36 and is the same as the one obtained by the intermediate-waveform method in Example 5–14. The corresponding product terms for each waveform condition that results in a HIGH output are indicated.

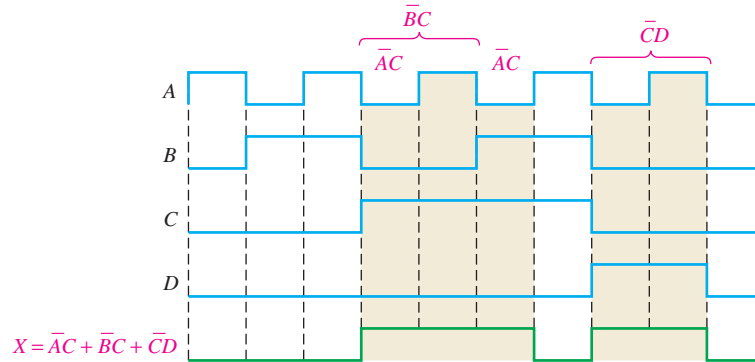


FIGURE 5-36

Related Problem

Repeat this example if all the input waveforms are inverted.

SECTION 5-5 CHECKUP

1. One pulse with $t_W = 50 \mu s$ is applied to one of the inputs of an exclusive-OR circuit. A second positive pulse with $t_W = 10 \mu s$ is applied to the other input beginning $15 \mu s$ after the leading edge of the first pulse. Show the output in relation to the inputs.
2. The pulse waveforms A and B in Figure 5–31 are applied to the exclusive-NOR circuit in Figure 5–32. Develop a complete timing diagram.