Example 13-4

A 2N5459 has $V_{GS(off)} = -8$ V and $I_{DSS} = 16$ mA. What is the drain current at the half cutoff point?

SOLUTION The drain current is one quarter of the maximum, or:

$$I_D = 4 \text{ mA}$$

The gate-source voltage that produces this current is -4 V, half of the cutoff voltage.

PRACTICE PROBLEM 13-4 Repeat Example 13-4 using a JFET with $V_{GS(off)} = -6$ V and $I_{DSS} = 12$ mA.

13-4 Biasing in the Ohmic Region

The JFET can be biased in the ohmic or in the active region. When biased in the ohmic region, the JFET is equivalent to a resistance. When biased in the active region, the JFET is equivalent to a current source. In this section, we discuss gate bias, the method used to bias a JFET in the ohmic region.

Gate Bias

Figure 13-7*a* shows **gate bias.** A negative gate voltage of $-V_{GG}$ is applied to the gate through biasing resistor R_G. This sets up a drain current that is less than I_{DSS}. When the drain current flows through R_D, it sets up a drain voltage of:

$$V_D = V_{DD} - I_D R_D \tag{13-4}$$

Gate bias is the worst way to bias a JFET in the active region because the Q point is too unstable.

For example, a 2N5459 has the following spreads between minimum and maximum: I_{DSS} varies from 4 to 16 mA, and $V_{GS(off)}$ varies from -2 to -8 V. Figure 13-7*b* shows the minimum and maximum transconductance curves. If a gate bias of -1 V is used with this JFET, we get the minimum and maximum Q points shown. Q_1 has a drain current of 12.3 mA, and Q_2 has a drain current of only 1 mA.

Hard Saturation

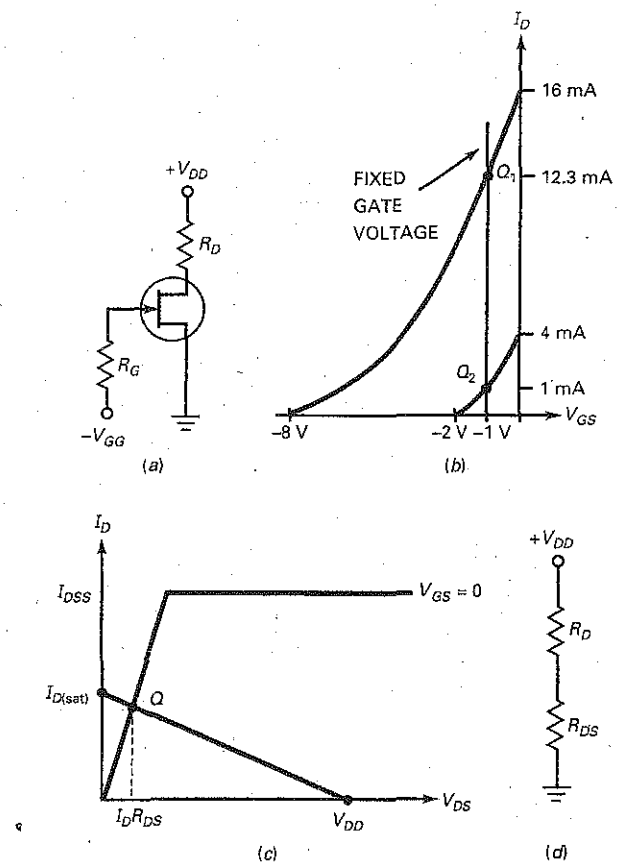
Although not suitable for active-region biasing, gate bias is perfect for ohmic-region biasing because stability of the Q point does not matter. Figure 13-7*c* shows how to bias a JFET in the ohmic region. The upper end of the dc load line has a drain saturation current of:

$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

To ensure that a JFET is biased in the ohmic region, all we need to do is use $V_{GS} = 0$ and:

$$I_{D(sat)} \ll I_{DSS} \tag{13-5}$$

Figure 13-7 (*a*) Gate bias; (*b*) *Q* point unstable in active region; (*c*) biased in ohmic region; (*d*) JFET is equivalent to resistance.



The symbol $\ll$ means "much less than." This equation says that the drain saturation current must be much less than the maximum drain current. For instance, if a JFET has $I_{DSS} = 10$ mA, hard saturation will occur if $V_{GS} = 0$ and $I_{D(sat)} = 1$ mA.

When a JFET is biased in the ohmic region, we can replace it by a resistance of R_{DS}, as shown in Fig. 13-7*d*. With this equivalent circuit, we can calculate the drain voltage. When R_{DS} is much smaller than R_D, the drain voltage is close to zero.

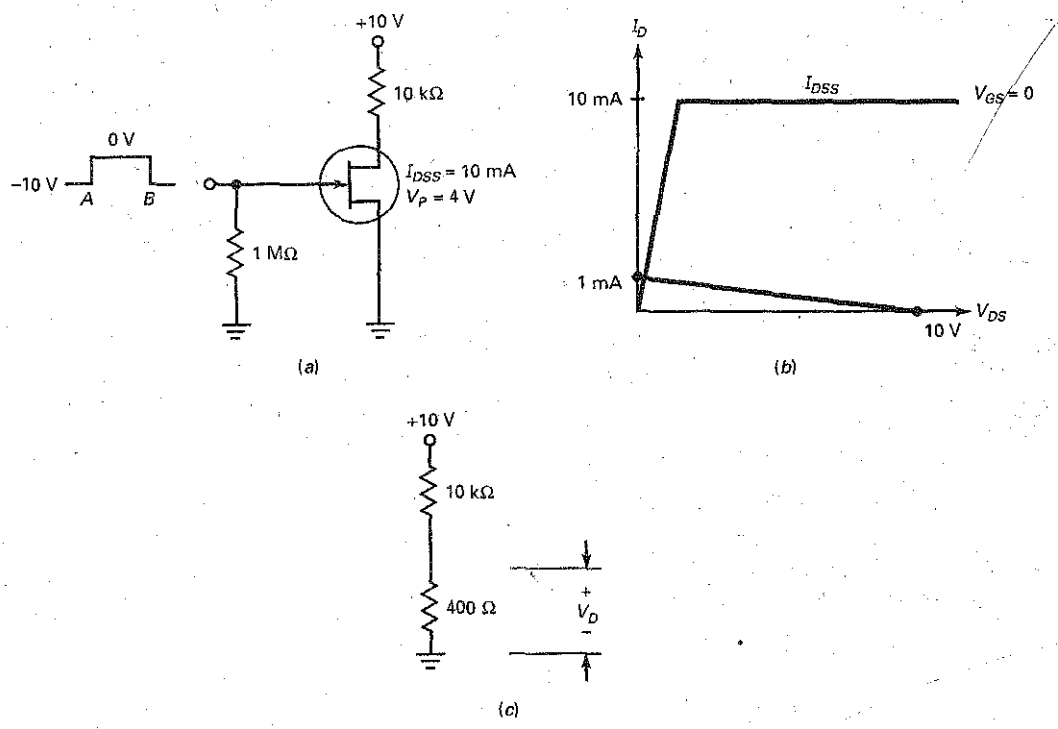
Example 13-5

What is the drain voltage in Fig. 13-8*a*?

SOLUTION Since $V_P = 4$ V, $V_{GS(off)} = -4$ V. Before point *A* in time, the input voltage is -10 V and the JFET is cut off. In this case, the drain voltage is:

$$V_D = 10 \text{ V}$$

Figure 13-8 Example.



Between points A and B, the input voltage is 0 V. The upper end of the dc load line has a saturation current of:

$$I_{D(sat)} = \frac{10\text{ V}}{10\text{ k}\Omega} = 1\text{ mA}$$

Figure 13-8*b* shows the dc load line. Since $I_{D(sat)}$ is much less than I_{DSS}, the JFET is in hard saturation.

The ohmic resistance is:

$$R_{DS} = \frac{4\text{ V}}{10\text{ mA}} = 400\ \Omega$$

In the equivalent circuit of Fig. 13-8*c*, the drain voltage is:

$$V_D = \frac{400\ \Omega}{10\text{ k}\Omega + 400\ \Omega}10\text{ V} = 0.385\text{ V}$$

PRACTICE PROBLEM 13-5 Using Fig. 13-8*a*, find R_{DS} and V_D if $V_p = 3$ V.