13-5 Biasing in the Active Region

JFET amplifiers need to have a Q point in the active region. Because of the large spread in JFET parameters, we cannot use gate bias. Instead, we need to use other biasing methods. Some of these methods are similar to those used with bipolar junction transistors.

The choice of analysis technique depends on the level of accuracy needed. For example, when doing preliminary analysis and troubleshooting of biasing circuits, it is often desirable to use ideal values and circuit approximations. In JFET circuits, this means that we will often ignore V_{GS} values. Usually, the ideal answers will have an error of less that 10 percent. When closer analysis is called for, we can use graphical solutions to determine a circuit's Q point. If you are designing JFET circuits or need even greater accuracy, you should use a circuit simulator like MultiSim (EWB).

Self-Bias

Figure 13-9*a* shows **self-bias.** Since drain current flows through the source resistor R_S, a voltage exists between the source and ground, given by:

$$V_S = I_D R_S \tag{13-6}$$

Since V_G is zero,

$$V_{GS} = -I_D R_S \tag{13-7}$$

This says that the gate-source voltage equals the negative of the voltage across the source resistor. Basically, the circuit creates its own bias by using the voltage developed across R_S to reverse bias the gate.

Figure 13-9*b* shows the effect of different source resistors. There is a medium value of R_S at which the gate-source voltage is half of the cutoff voltage. An approximation for this medium resistance is:

$$R_S \approx R_{DS} \tag{13-8}$$

This equation says that the source resistance should equal the ohmic resistance of the JFET. When this condition is satisfied, the V_{GS} is roughly half the cutoff voltage and the drain current is roughly one-quarter of I_{DSS}.

Figure 13-9 Self-bias.

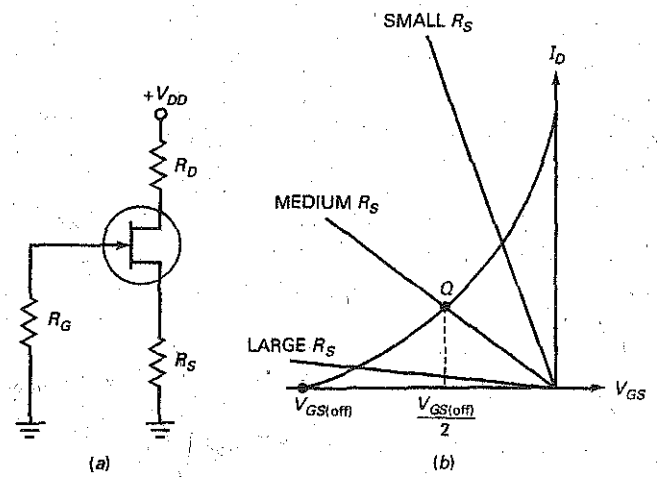
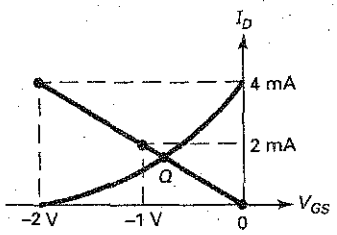


Figure 13-10 Self-bias Q point.



When a JFET's transconductance curves are known, we can analyze a self-bias circuit using graphical methods. Suppose a self-bias JFET has the transconductance curve shown in Fig. 13-10. The maximum drain current is 4 mA, and the gate voltage has to be between 0 and −2 V. By graphing Eq. (13-7), we can find out where it intersects the transconductance curve and determine the values of V_{GS} and I_D. Since Eq. (13-7) is a linear equation, all we have to do is plot two points and draw a line through them.

Suppose the source resistance is 500 Ω. Then Eq. (13-7) becomes:

$$V_{GS} = -I_D\,(500\ \Omega)$$

Since any two points can be used, we choose the two convenient points corresponding to $I_D = -(0)(500\ \Omega) = 0$, therefore, the coordinates for the first point are (0, 0), which is the origin. To get the second point, find V_{GS} for $I_D = I_{DSS}$. In this case, $I_D = 4$ mA and $V_{GS} = -(4\text{ mA})(500\ \Omega) = -2$ V, therefore, the coordinates of the second point are at (4 mA, −2 V).

We now have two points on the graph of Eq. (13-7). The two points are (0, 0) and (4 mA, −2 V). By plotting these two points as shown in Fig. 13-10, we can draw a straight line through the two points as shown. This line will, of course, intersect the transconductance curve. This intersection point is the operating point of the self-biased JFET. As you can see, the drain current is slightly less than 2 mA, and the gate-source voltage is slightly less than −1 V.

In summary, here is a process for finding the Q point of any self-biased JFET, provided you have the transconductance curve. If the curve is not available, you can use the $V_{GS(off)}$ and I_{DSS} rated values, along with the square law equation (13-3), to develop one:

1. Multiply I_{DSS} by R_S to get V_{GS} for the second point.
2. Plot the second point (I_{DSS}, V_{GS}).
3. Draw a line through the origin and the second point.
4. Read the coordinates of the intersection point.

The Q point with self-bias is not extremely stable. Because of this, self-bias is used only with small-signal amplifiers. This is why you may see self-biased JFET circuits near the front end of communication receivers where the signal is small.

Example 13-6

In Fig. 13-11*a*, what is a medium source resistance using the rule discussed earlier? Estimate the drain voltage with this source resistance.

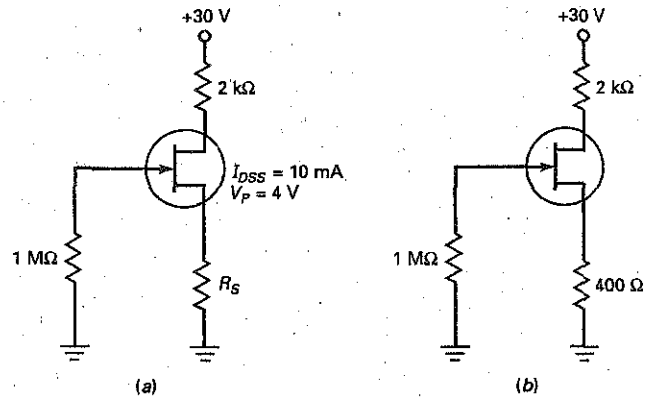
SOLUTION As discussed earlier, self-bias works fine if you use a source resistance equal to the ohmic resistance of the JFET:

$$R_{DS} = \frac{4\text{ V}}{10\text{ mA}} = 400\ \Omega$$

Figure 13-11*b* shows a source resistance of 400 Ω. In this case, the drain current is around one-quarter of 10 mA, or 2.5 mA, and the drain voltage is roughly:

$$V_D = 30\text{ V} - (2.5\text{ mA})(2\text{ k}\Omega) = 25\text{ V}$$

Figure 13–11 Example.



PRACTICE PROBLEM 13–6 Repeat Example 13-6 using a JFET with $I_{DSS} = 8$ mA. Determine R_S and V_D.

Example 13–7

MultiSim

Using the MultiSim circuit of Fig. 13-12*a*, along with the minimum and maximum transconductance curves for a 2N5486 JFET shown in Fig. 13-12*b*, determine the range of V_{GS} and I_D Q point values. Also, what would be the optimum source resistor for this JFET?

SOLUTION First, multiply I_{DSS} by R_S to get V_{GS}:

$$V_{GS} = -(20 \text{ mA})(270\ \Omega) = -5.4 \text{ V}$$

Second, plot the second point (I_{DSS}, V_{GS}):

(20 mA, −5.4 V)

Now draw a line through the origin (0, 0) and the second point. Then read the coordinates of the intersection points for the minimum and maximum Q point values.

Q point (min) $V_{GS} = -0.8$ V $I_D = 2.8$ mA
Q point (max) $V_{GS} = -2.1$ V $I_D = 8.0$ mA

Note that the MultiSim measured values of Fig. 13-12*a* are between the minimum and maximum values. The optimum source resistor can be found by:

$$R_S = \frac{V_{GS(off)}}{I_{DSS}} \quad \text{or} \quad R_S = \frac{V_P}{I_{DSS}}$$

using minimum values:

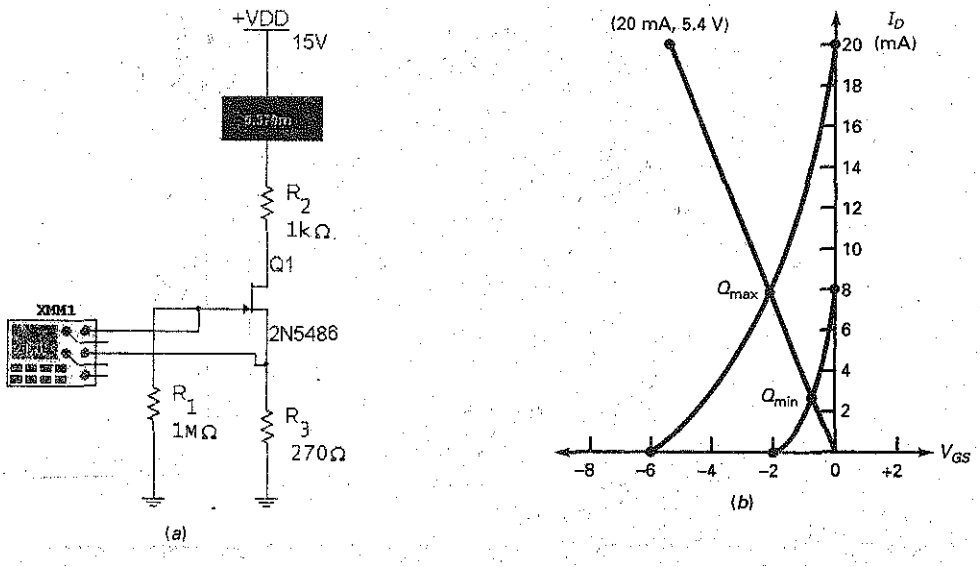
$$R_S = \frac{2 \text{ V}}{8 \text{ mA}} = 250\ \Omega$$

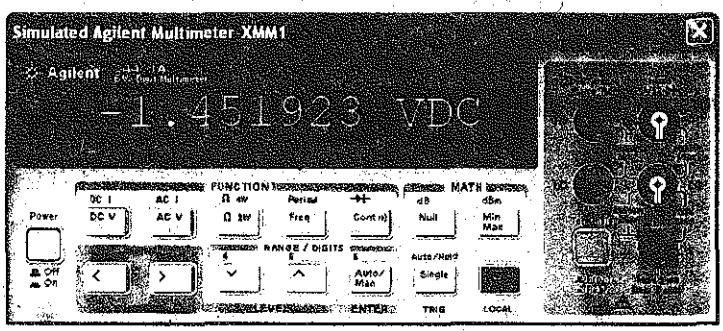
using maximum values:

$$R_S = \frac{6 \text{ V}}{20 \text{ mA}} = 300\ \Omega$$

Notice the value of R_S in Fig. 13-12*a* is an approximate midpoint value between $R_{S(min)}$ and $R_{S(max)}$.

Figure 13-12 (*a*) Self-bias example; (b) transconductance curves.





PRACTICE PROBLEM 13-7 In Fig. 13-12*a*, change R_S to 390 Ω and find the Q point values.

Voltage-Divider Bias

Figure 13-13*a* shows **voltage-divider bias.** The voltage divider produces a gate voltage that is a fraction of the supply voltage. By subtracting the gate-source voltage, we get the voltage across the source resistor:

$$V_S = V_G - V_{GS} \tag{13-9}$$