GOOD TO KNOW

In general, JFETs are more temperature stable than bipolar transistors. Furthermore, JFETs are typically much smaller than bipolar transistors. This size difference makes them particularly suitable for use in ICs, where the size of each component is very critical.

13–1 Basic Ideas

Figure 13-1*a* shows a piece of *n*-type semiconductor. The lower end is called the **source,** and the upper end is called the **drain.** The supply voltage V_{DD} forces free electrons to flow from the source to the drain. To produce a JFET, a manufacturer diffuses two areas of *p*-type semiconductor into the *n*-type semiconductor, as shown in Fig. 13-1*b*. These *p* regions are connected internally to get a single external **gate** *lead.*

Field Effect

Figure 13-2 shows the normal biasing voltages for a JFET. The drain supply voltage is positive, and the gate supply voltage is negative. The term **field effect** is related to the depletion layers around each *p* region. These depletion layers exist because free electrons diffuse from the *n* regions into the *p* regions. The recombination of free electrons and holes creates the depletion layers shown by the colored areas.

Reverse Bias of Gate

In Fig. 13-2, the *p*-type gate and the *n*-type source form the gate-source diode. With a JFET, we always *reverse-bias* the gate-source diode. Because of reverse bias, the gate current I_G is approximately zero, which is equivalent to saying that the JFET has an almost infinite input resistance.

Figure 13–1 (*a*) Part of JFET; (*b*) single-gate JFET.

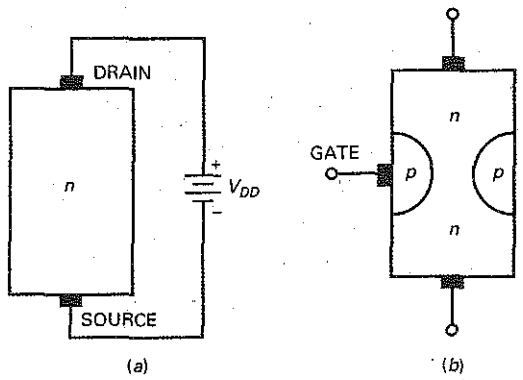
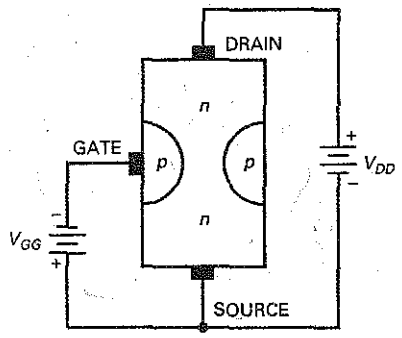


Figure 13–2 Normal biasing of JFET.



A typical JFET has an input resistance in the hundreds of megohms. This is the big advantage that a JFET has over a bipolar transistor. It is the reason that JFETs excel in applications in which a high input impedance is required. One of the most important applications of the JFET is the *source follower*, a circuit like the emitter follower, except that the input impedance is in the hundreds of megohms for lower frequencies.

Gate Voltage Controls Drain Current

In Fig. 13-2, electrons flowing from the source to the drain must pass through the narrow **channel** between the depletion layers. When the gate voltage becomes more negative, the depletion layers expand and the conducting channel becomes narrower. The more negative the gate voltage, the smaller the current between the source and the drain.

The JFET is a **voltage-controlled device** because an input voltage controls an output current. In a JFET, the gate-to-source voltage V_{GS} determines how much current flows between the source and the drain. When V_{GS} is zero, maximum drain current flows through the JFET. This is why a JFET is referred to as a normally on device. On the other hand, if V_{GS} is negative enough, the depletion layers touch and the drain current is cut off.

GOOD TO KNOW

The depletion layers are actually wider near the top of the *p*-type materials and narrower at the bottom. The reason for the change in the width can be understood by realizing that the drain current I_D will produce a voltage drop along the length of the channel. With respect to the source, a more positive voltage is present as you move up the channel toward the drain end. Since the width of a depletion layer is proportional to the amount of reverse-bias voltage, the depletion layer of the *pn* junction must be wider at the top, where the amount of reverse-bias voltage is greater.

Schematic Symbol

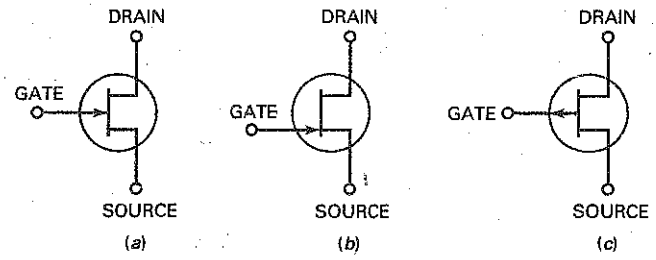
The JFET of Fig. 13-2 is an *n-channel JFET* because the channel between the source and the drain is an *n*-type semiconductor. Figure 13-3*a* shows the schematic symbol for an *n*-channel JFET. In many low-frequency applications, the source and the drain are interchangeable because you can use either end as the source and the other end as the drain.

The source and drain terminals are not interchangeable at high frequencies. Almost always, the manufacturer minimizes the internal capacitance on the drain side of the JFET. In other words, the capacitance between the gate and the drain is smaller than the capacitance between the gate and the source. You will learn more about internal capacitances and their effect on circuit action in a later chapter.

Figure 13-3*b* shows an alternative symbol for an *n*-channel JFET. This symbol with its offset gate is preferred by many engineers and technicians. The offset gate points to the source end of the device, a definite advantage in complicated multistage circuits.

There is also a *p*-channel JFET. The schematic symbol for a *p*-channel JFET, shown in Fig. 13-3*c*, is similar to that for the *n*-channel JFET, except that the gate arrow points in the opposite direction. The action of a *p*-channel JFET is complementary; that is, all voltages and currents are reversed. To reverse bias a *p*-channel JFET, the gate is made positive in respect to the source. Therefore, V_{GS} is made positive.

Figure 13-3 (*a*) Schematic symbol; (*b*) offset-gate symbol; (*c*) *p*-channel symbol.



Example 13–1

A 2N5486 JFET has a gate current of 1 nA when the reverse gate voltage is 20 V. What is the input resistance of this JFET?

SOLUTION Use Ohm's law to calculate:

$$R_{in} = \frac{20\text{ V}}{1\text{ nA}} = 20{,}000\text{ M}\Omega$$

PRACTICE PROBLEM 13–1 In Example 13-1, calculate the input resistance if the JFET's gate current is 2 nA.

13–2 Drain Curves

Figure 13-4*a* shows a JFET with normal biasing voltages. In this circuit, the gate-source voltage V_{GS} equals the gate supply voltage V_{GG}, and the drain-source voltage V_{DS} equals the drain supply voltage V_{DD}.

Maximum Drain Current

If we short the gate to the source, as shown in Fig. 13-4*b*, we will get maximum drain current because $V_{GS} = 0$. Figure 13-4*c* shows the graph of drain current I_D versus drain-source voltage V_{DS} for this shorted-gate condition. Notice how the drain current increases rapidly and then becomes almost horizontal when V_{DS} is greater than V_P.

GOOD TO KNOW

The pinchoff voltage V_P is the point at which further increases in V_{DS} are offset by a proportional increase in the channel's resistance. This means that if the channel resistance is increasing in direct proportion to V_{DS} above V_P, I_D must remain the same above V_P.

Figure 13-4 (*a*) Normal bias; (*b*) zero gate voltage; (*c*) shorted gate drain current.