Program: BC (CS)

Subject: Digital Logic Design

Assignment Number: 08

Course Code: CSC-201

EDP Code: 102002077

Spring Semester 2020

Q.1 For the ripple counter shown in Figure 01, show the complete timing diagram for four clock pulses, showing the clock, Q_0, and Q_1 waveforms.

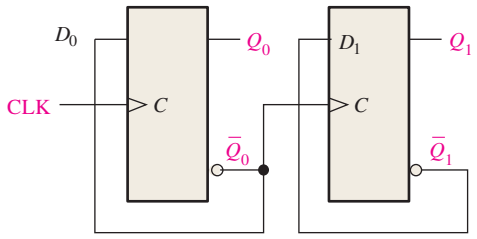

FIGURE 01

Q.2 For the ripple counter in Figure 02, show the complete timing diagram for eight clock pulses. Show the clock, Q_0, Q_1, and Q_2 waveforms.

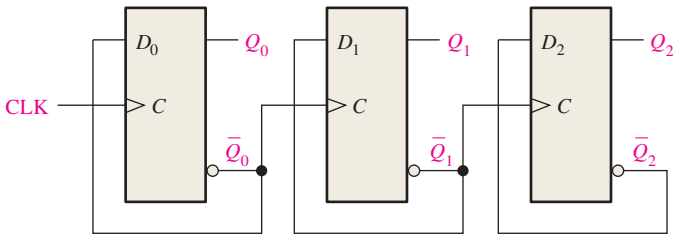

FIGURE 02

Q.3 In the counter of Q.2, assume that each flip-flop has a propagation delay from the triggering edge of the clock to a change in the Q output of 8 ns. Determine the worst-case (longest) delay time from a clock pulse to the arrival of the counter in a given state. Specify the state or states for which this worst-case delay occurs.

Q.4 If the counter of Q.3 were synchronous rather than asynchronous, what would be the longest delay time?

Q.5 Show the complete timing diagram for the 5-stage synchronous binary counter in Figure 03. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

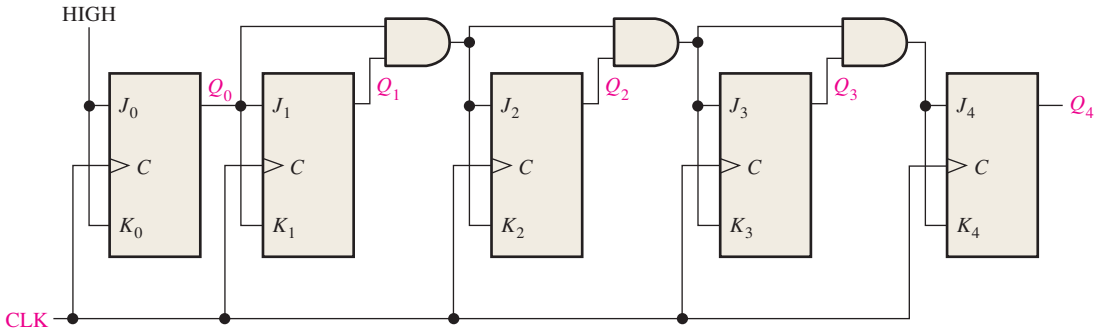

FIGURE 03