



Program: BC (CS)

Subject: Digital Logic Design

Assignment Number: 07

Course Code: CSC-201

EDP Code: 102002077

Spring Semester 2020

- Q.1** What is a register?
- Q.2** What is the storage capacity of a register that can retain one byte of data?
- Q.3** What does the “shift capacity” of a register mean?
- Q.4** The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared. What is the state of the shift register after three clock pulses?
- Q.5** For the data input and clock in Figure 01 (a), determine the states of each flip-flop in the shift register of Figure 01 (b) and show the Q waveforms. Assume that the register contains all 1s initially.

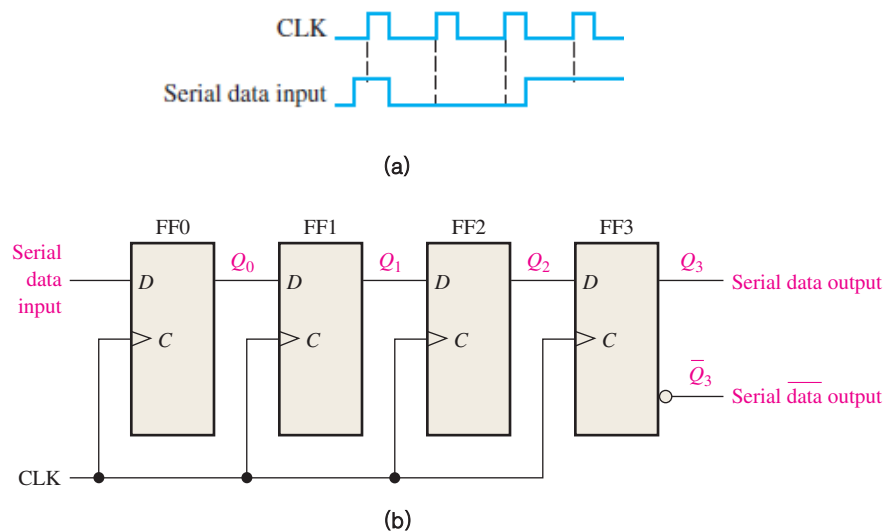


FIGURE 01

- Q.6** What is the state of the register in Figure 02 after each clock pulse if it starts in the 110001110000 state?

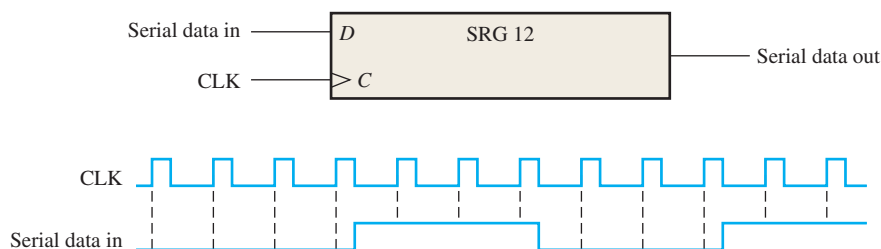


FIGURE 02

- Q.7** For the serial in/serial out shift register, determine the data-output waveform for the data-input and clock waveforms in Figure 03. Assume that the register is initially cleared.

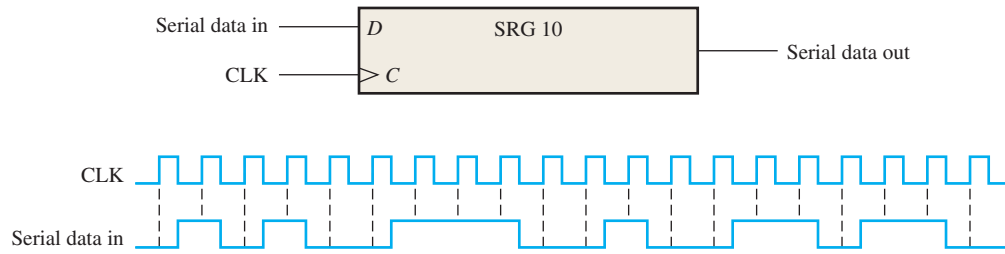


FIGURE 03

- Q.8** A leading-edge clocked serial in/serial out shift register has a data-output waveform as shown in Figure 04. What binary number is stored in the 8-bit register if the first data bit out (left-most) is the LSB?

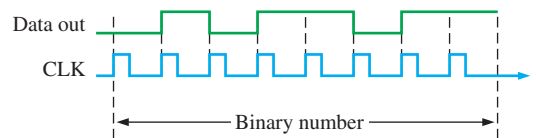


FIGURE 04

- Q.9** Show a complete timing diagram including the parallel outputs for the shift register in Figure 05. Use the waveforms in Figure 05 (c) with the register initially clear.

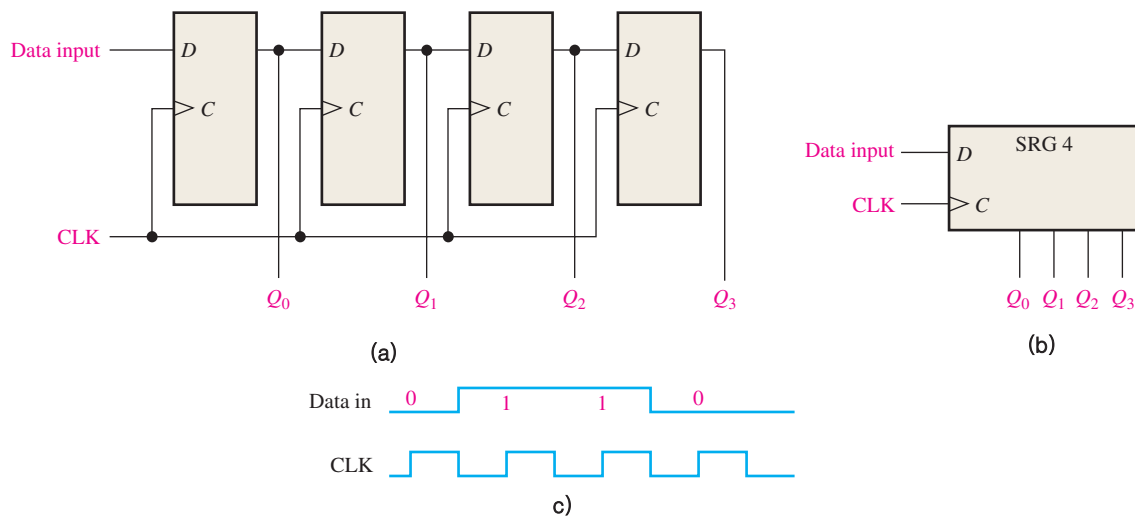


FIGURE 05

- Q.10** The shift register in Figure 06 (a) has $\overline{SHIFT/LOAD}$ and CLK inputs as shown in part (b). The serial data input (SER) is a 0. The parallel data inputs are $D_0 = 1$, $D_1 = 0$, $D_2 = 1$, and $D_3 = 0$ as shown. Develop the data-output waveform in relation to the inputs.

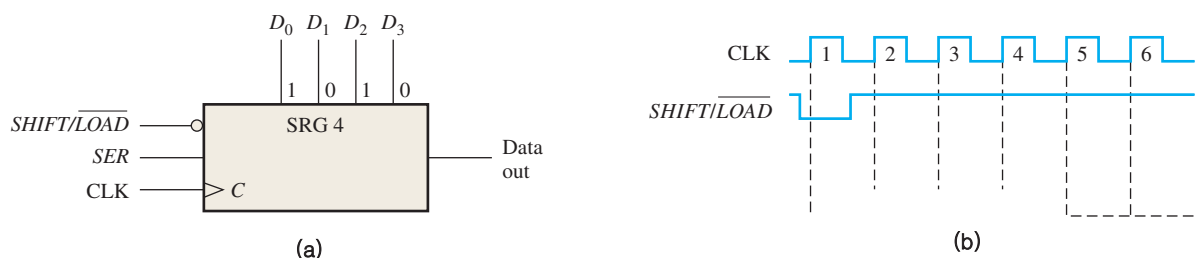


FIGURE 06