Assignment No. 06
Digital Logic Design
BC (SE) & BS (CS)
Spring Semester 2018

Q.1 If the waveforms in Figure 01 are applied to an active-HIGH S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW.

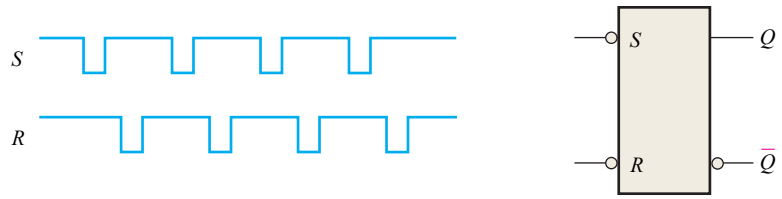

FIGURE 01

Q.2 Solve Q.1 for the input waveforms in Figure 02 applied to an active-LOW $\overline{S} - \overline{R}$ latch.

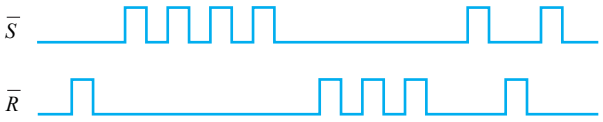

FIGURE 02

Q.3 For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure 03. Show them in proper relation to the enable input. Assume that Q starts LOW.

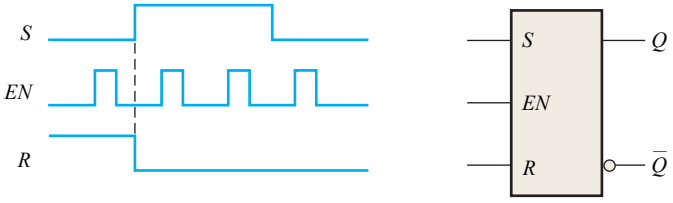

FIGURE 03

Q.4 Determine the output of a gated D latch for the inputs in Figure 04.

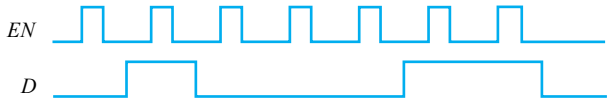

FIGURE 04

Q.5 Two edge-triggered J-K flip-flops are shown in Figure 05. If the inputs are as shown, draw the *Q* output of each flip-flop relative to the clock, and explain the difference between the two. The flip-flops are initially RESET.

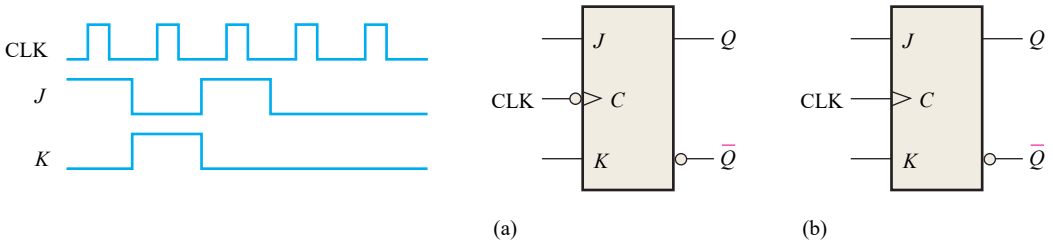

FIGURE 05

Q.6 The *Q* output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 06. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

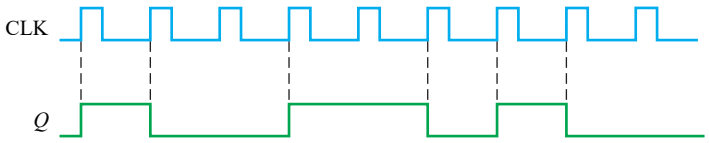

FIGURE 06

Q.7 Draw the *Q* output relative to the clock for a D flip-flop with the inputs as shown in Figure 07. Assume positive edge-triggering and *Q* initially LOW.

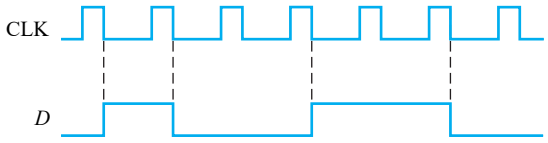

FIGURE 07

Q.8 Solve Q.7 for the inputs in Figure 08.

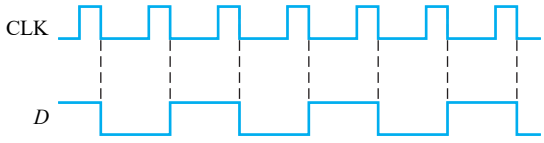

FIGURE 08

Q.9 For a positive edge-triggered D flip-flop with the input as shown in Figure 09, determine the *Q* output relative to the clock. Assume that *Q* starts LOW.

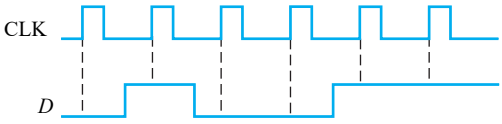

FIGURE 09

Q.10 Solve Q.9 for the input in Figure 10.

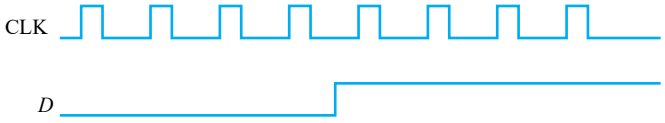

FIGURE 10

Q.11 Determine the Q waveform relative to the clock if the signals shown in Figure 11 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

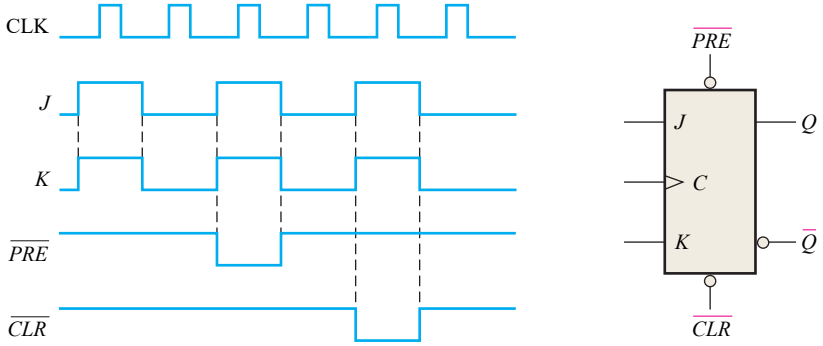

FIGURE 11

Q.12 For a negative edge-triggered J-K flip-flop with the inputs in Figure 12, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

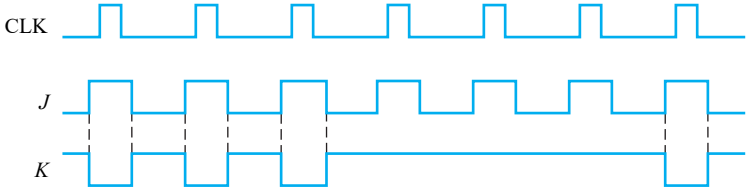

FIGURE 12

Q.13 The following serial data are applied to the flip-flop through the AND gates as indicated in Figure 13. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that $\overline{PRE}$ and $\overline{CLR}$ are HIGH. Right-most bits are applied first.

J_1: 1 0 1 0 0 1 1; J_2: 0 1 1 1 0 1 0; J_3: 1 1 1 1 0 0 0; K_1: 0 0 0 1 1 1 0; K_2: 1 1 0 1 1 0 0;

K_3: 1 0 1 0 1 0 1

Q.14 For the circuit in Figure 13, complete the timing diagram in Figure 14 by showing the Q output (which is initially LOW). Assume $\overline{PRE}$ and $\overline{CLR}$ remain HIGH.

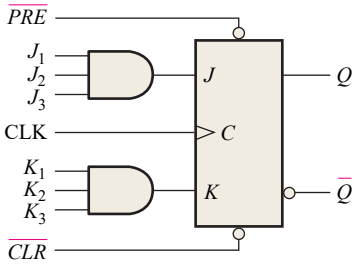

FIGURE 13

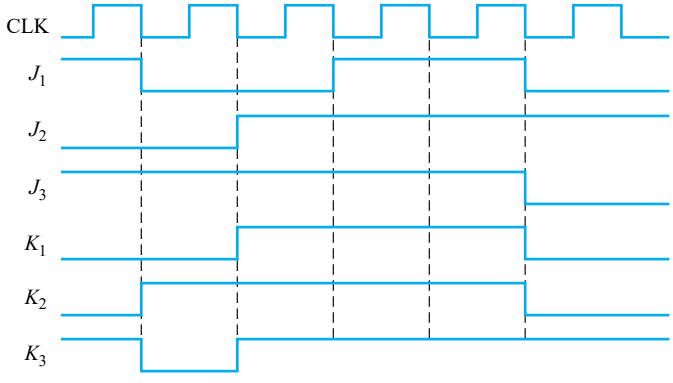

FIGURE 14

Q.15 Solve Q.14 with the same J and K inputs but with the $\overline{PRE}$ and $\overline{CLR}$ inputs as shown in Figure 15 in relation to the clock.

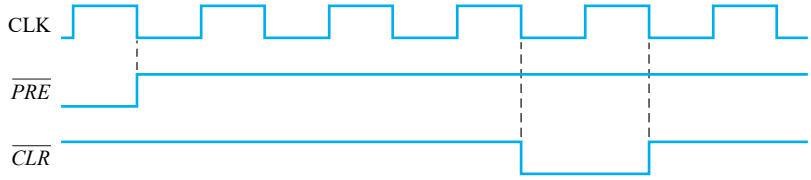

FIGURE 15

Q.16 For the circuit in Figure 16, develop a timing diagram for eight clock pulses, showing the Q_A and Q_B outputs in relation to the clock.

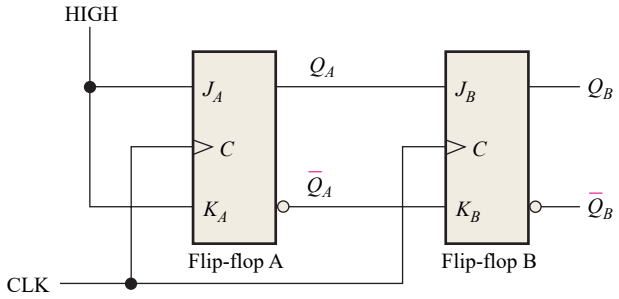

FIGURE 16

Q17 A D flip-flop is connected as shown in Figure 17. Determine the Q output in relation to the clock. What specific function does this device perform?

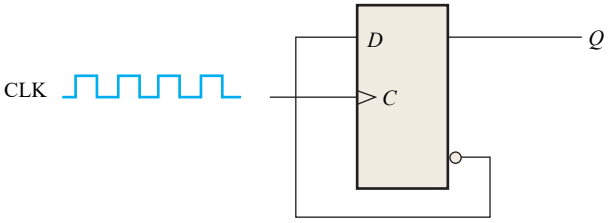

FIGURE 17

Q18 Draw a logic diagram that can store 4 bits of data from parallel lines simultaneously using D-flip-flops. Also use the asynchronous reset inputs $\overline{CLR}$ lines to reset all the flip-flops initially.

Q19 Draw a logic diagram that can divide the frequency of a periodic wave-form using 3 J-K flip-flops. Suppose the frequency of the initial wave-form is 8 kHz. The circuit must produce the output wave-forms each having 4 kHz, 2 kHz, and 1 kHz frequencies.