Program: BC (CS)

Subject: Digital Logic Design

Assignment Number: 05

Course Code: CSC-201

EDP Code: 101902015

Spring Semester 2019

Q.1 Determine the outputs of a full-adder for the following inputs: $A = 1, B = 0, C_{in} = 1$

Q.2 What are the half-adder inputs that will produce the following output: $\Sigma = 0$, Cout = 0

Q.3 Determine the outputs of a full-adder for the following inputs: $A = 1$, B = 1, Cin = 1

Q.4 For the parallel adder in Figure 01, determine the complete sum by analysis of the logical operation of the circuit. Verify your result by longhand addition of the two input numbers.

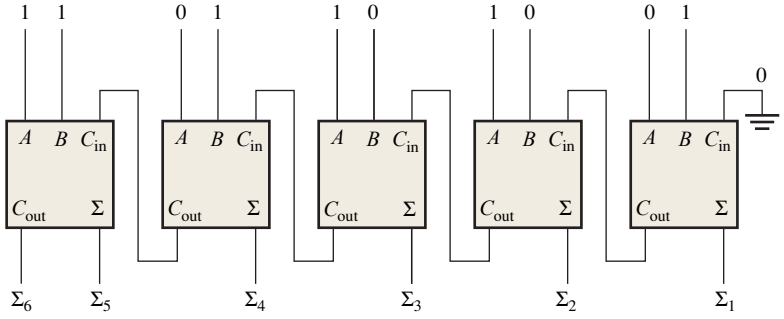


FIGURE 01

Q.5 The circuit shown in Figure 02 is a 4-bit circuit that can add or subtract numbers in a form used in computers (positive numbers in true form; negative numbers in complement form). (a) Explain what happens when the $\overline{Add}/Subt.$ input is HIGH. (b) What happens when $\overline{Add}/Subt.$ is LOW?

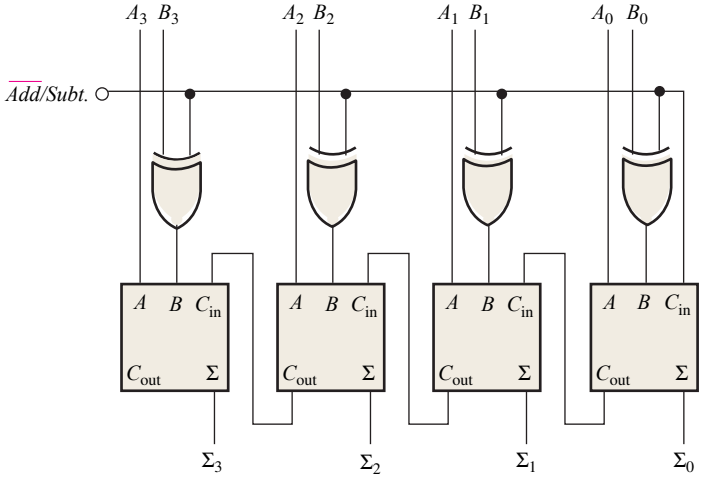


FIGURE 02

Q.6 For the circuit in Figure 02 , assume the inputs are $\overline{Add}/Subt. = 1$, $A = 1010$, and B = 1101. What is the output?

Q.7 The input waveforms in Figure 03 are applied to a 2-bit adder. Determine the waveforms for the sum and the output carry in relation to the inputs by constructing a timing diagram.

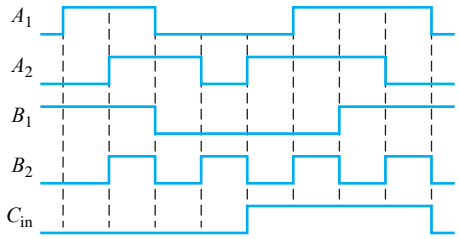


FIGURE 03

Q.8 The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

Q.9 Draw the logic circuitry necessary for a 02-bit look-ahead carry adder.

Q.10 For the 4-bit comparator in Figure 04, plot each output waveform for the inputs shown. The outputs are active-HIGH.

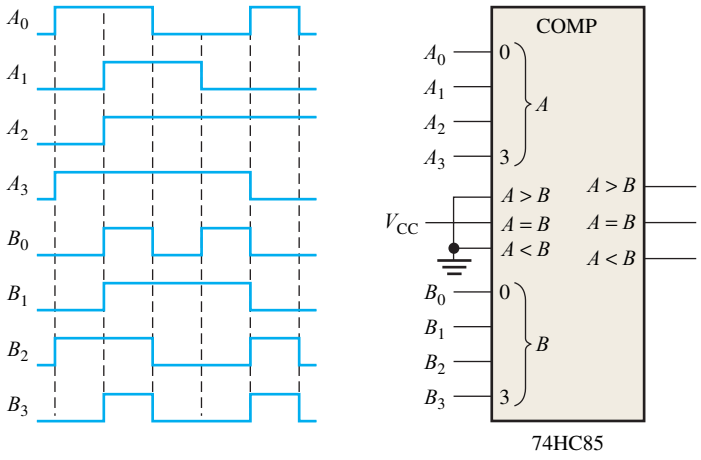


FIGURE 04

Q.11 Show the decoding logic for the following codes if an active-HIGH (1) output is required: 1110110

Q.12 Draw logic diagram for 2 to 4 line decoder.

Q.13 A 7-segment decoder/driver drives the display in Figure 05. If the waveforms are applied as indicated, determine the sequence of digits that appears on the display.

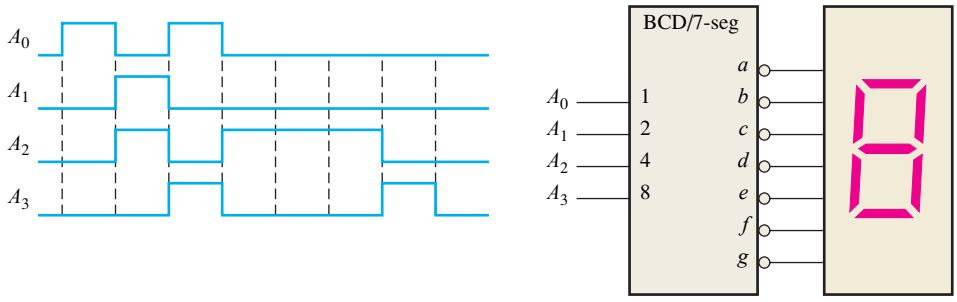


FIGURE 05

Q.14 Draw logic diagram for decimal to BCD encoder.

Q.15 Show the logic required to convert a 5-bit binary number to Gray code and use that logic to convert the following binary numbers to Gray code: 10100

Q.16 Show the logic required to convert a 5-bit Gray code to binary and use that logic to convert the following Gray code words to binary: 10111

Q.17 For the multiplexer in Figure 06, determine the output for the following input states: D0 = 1, D1 = 0, D2 = 0, D3 = 1, S0 = 0, S1 = 1.

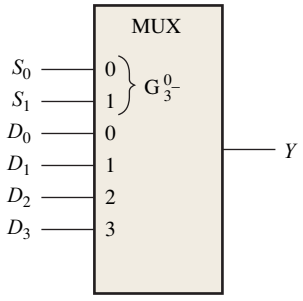


FIGURE 06

Q.18 If the data-select inputs to the multiplexer in Figure 06 are sequenced as shown by the wave-forms in Figure 07, determine the output waveform with the data inputs specified in Q.17.

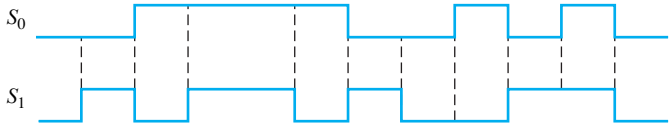


FIGURE 07

Q.19 Draw logic diagram for 4 to 1 line multiflexer.

Q.20 Draw logic diagram for 1 to 4 line de-multiflexer.

Q.21 The waveforms in Figure 08 are applied to the 4-bit parity logic. Determine the output wave-form in proper relation to the inputs. For how many bit times does even parity occur, and how is it indicated? The timing diagram includes eight bit times.

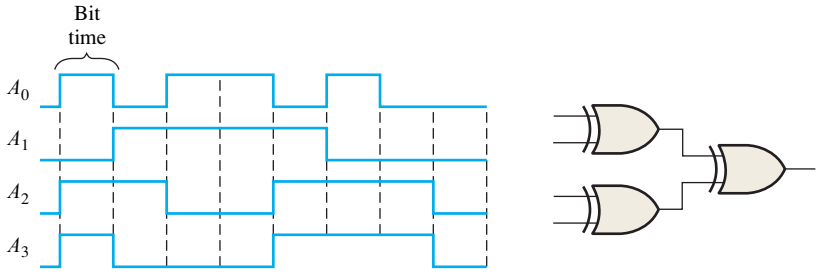
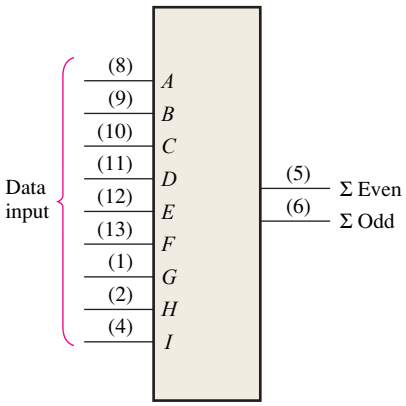


FIGURE 08

Q.22 Figure 09 shows the pin diagram and function table for the 74HC280 9-bit parity generator/checker. Determine the Σ Even and the Σ Odd outputs of a 74HC280 9-bit parity generator/checker for the inputs in Figure 10.



(a) Traditional logic symbol

Number of Inputs *A–I* that Are High	Outputs Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

(b) Function table

FIGURE 09

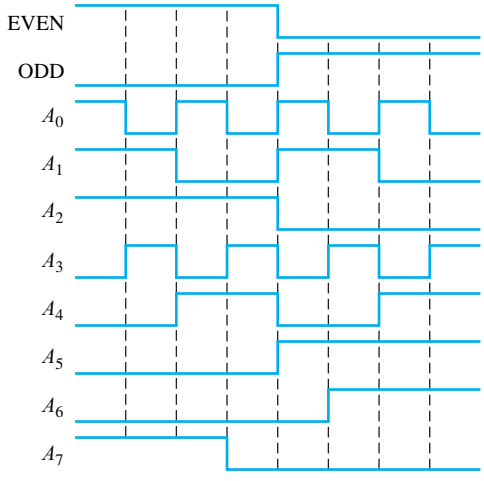


FIGURE 10

Q.23 Using 04 full adders, 02 parallel binary adders, 01 BCD to 7-segemnt decoder, and 01 7-segment display, design a simple voting system that can be used to simultaneously provide the number of "yes" votes and the number of "no" votes from 06 persons.