



Program: BC (CS)
Subject: Computer Architecture
Assignment Number: 04
Course Code: CSC-208
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Q.1 Give answers to each of the following:

- (i) What is the general relationship among access time, memory cost, and capacity?
- (ii) Discuss different Memory access methods in detail.
- (iii) Discuss the importance of memory hierarchy.
- (iv) How does the principle of locality relate to the use of multiple memory levels?
- (v) How main memory address is interpreted in direct, associative, and set-associative mapping?

Q.2 Write note on each of the following:

- (i) Memory unit of transfer
- (ii) Memory performance parameters
- (iii) Disk cache
- (iv) Principle of locality
- (v) Logical cache and physical cache
- (vi) Replacement algorithms
- (vii) Possible approaches to cache coherency

Q.3 Differentiate each of the following:

- (i) Sequential, direct, and random access methods
- (ii) Direct, associative, and set-associative mapping
- (iii) Split cache and unified cache
- (iv) Write through and write back

Q.4 Solve each of the following:

- (i) Suppose that the processor has access to two levels of memory. Level-1 contains 1000 words and has an access time of 0.01 μ s; level-2 contains 100,000 words and has an access time of 0.1 μ s. Assume that if a word to be accessed is in level 1, then the processor accesses it directly. If it is in level 2, then the word is first transferred to level 1 and then accessed by the processor. Suppose 95% of the memory accesses are found in level 1. Then find the average time to access a word.
- (ii) A two-way set-associative cache has lines of 16 bytes and a total size of 8-kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.
- (iii) For the main memory address BBBBBBH, show the following information in hexadecimal format:
 - a. Tag, Line, and Word values for a direct-mapped cache
 - b. Tag and Word values for an associative cache
 - c. Tag, Set, and Word values for a two-way set-associative cache