Program: BC (SE)

Subject: Digital Logic Design (Theory)

Assignment Number: 04

Course Code: SEC-201

EDP Code: 101902103

Spring Semester 2019

Q.1 Write the output expression for circuit in Figure 01.

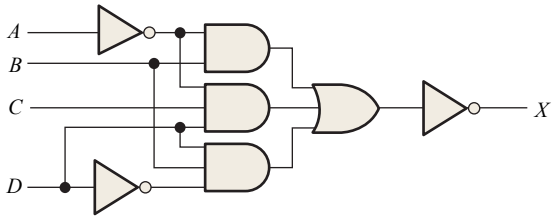

FIGURE 01

Q.2 Write the output expression for circuit as it appears in Figure 02 and then change it to an equivalent AND-OR configuration.

Q.3 Develop the truth table for circuit in Figure 02.

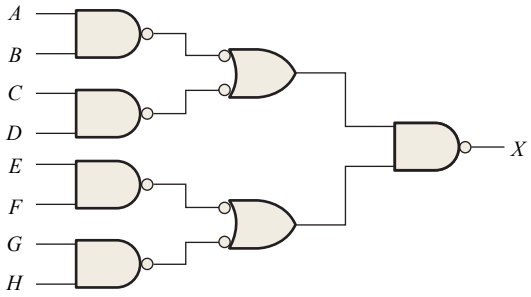

FIGURE 02

Q.4 Show that an exclusive-NOR circuit produces a POS output.

Q.5 Use AND gates, OR gates, or combinations of both to implement the following logic expressions as stated:

$$X = ABC(D + E + F) + AC(C + D + E)$$

Q.6 Use AND gates, OR gates, and inverters as needed to implement the following logic expres-sions as stated:

$$X ; \quad B(C\overline{D}E + \overline{E}FG)(\overline{AB} + C)$$

Q.7 Use NAND gates, NOR gates, or combinations of both to implement the following logic expressions as stated:

$$X = \overline{A}B + CD + \overline{(A + B)}\,(ACD + \overline{BE}$$

Q.8 Implement a logic circuit for the truth table in Table 01.

TABLE 01

Inputs				Output
A	***B***	***C***	***D***	***X***
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Q.9 Simplify the circuit in Figure 03 as much as possible, and verify that the simplified circuit is equivalent to the original by showing that the truth tables are identical.

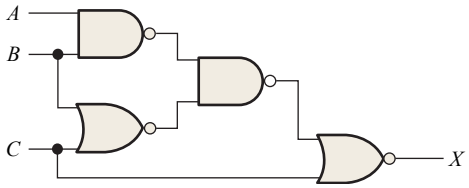

FIGURE 03

Q.10 Minimize the gates required to implement the function in Q.6 in SOP form.

Q.11 Minimize the gates required to implement the function in Q.7 in SOP form.

Q.12 Minimize the gates required to implement the function of the circuit in Figure 02 in SOP form.

Q.13 Implement the logic circuits in Figure 01 using only NAND gates.

Q.14 Implement the logic circuit in Figure 03 using only NAND gates.

Q.15 Repeat Q.13 using only NOR gates.

Q.16 Repeat Q.14 using only NOR gates.

Q.17 Show how the following expression can be implemented as stated using only NOR gates:

$$X = AB[C(\overline{DE} + \overline{AB}) + \overline{BCE}]$$

Q.18 Repeat Q.17 using only NAND gates.

Q.19 Implement the function in Q.5 by using only NAND gates.

Q.20 Implement the function in Q.6 by using only NAND gates.

Q.21 The output of the logic circuit and input waveforms in Figure 04 is passed through an inverter. Draw the output waveform.

FIGURE 04

Q.22 For the logic circuit in Figure 05, draw the output waveform in proper relationship to the inputs.

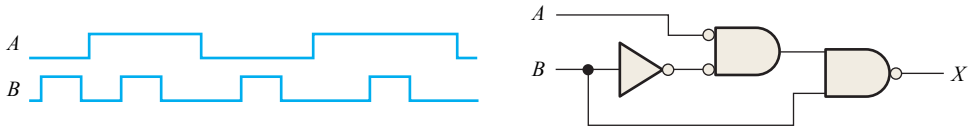

FIGURE 05

Q.23 For the input waveforms in Figure 06, what logic circuit will generate the output waveform shown?

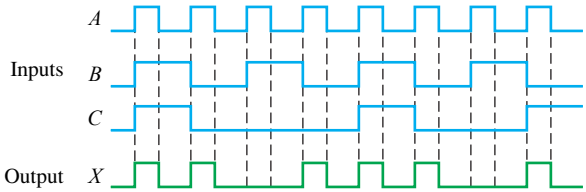

FIGURE 06

Q.24 For the circuit in Figure 07, draw the waveforms at the numbered points in the proper relationship to each other.

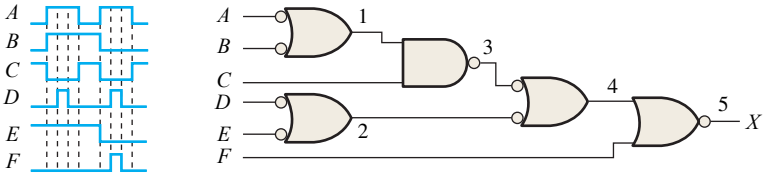

FIGURE 07