Program: BC (CS)

Subject: Computer Architecture

Assignment Number: 03

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Q.1 Give answer to each of the following:

- **A.** Discuss the two approaches for dealing with multiple interrupts.
- **B.** Discuss the types of exchanges that are needed by indicating the major forms of input and output for processor, memory, and I/O modules.
- **C.** Discuss the QuickPath Interconnect (QPI) protocol layers.
- **D.** Discuss the physical and Logical architecture of PCIe in detail.

Q.2 Write short note on each of the following**:**

- **A.** Instruction cycle
- **B.** Instruction cycle state diagram
- **C.** Classes of Interrupts
- **D.** Bus Interconnection Scheme

Q.3 Differentiate each of the following:

- **A.** Programing in hardware and programming in software
- **B.** Program flow of control without interrupt and with interrupt
- **C.** Disabled interrupt and nested interrupt processing

Q.4 Solve each of the following:

- **A.** The hypothetical machine of has two I/O instructions (see Figure 01):

  0011 = Load AC from I/O

  0111 = Store AC to I/O

  In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

Load AC from device 5.

Add contents of memory location 940.

Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

B. The program execution of Figure 02 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

C. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

- **a.** What is the maximum directly addressable memory capacity (in bytes)?
- **b.** Discuss the impact on the system speed if the microprocessor bus has:
  - **1.** 32-bit local address bus and a 16-bit local data bus, or
  - **2.** 16-bit local address bus and a 16-bit local data bus.
- **c.** How many bits are needed for the program counter and the instruction register?

D. Consider a 32-bit microprocessor, with a 16-bit external data bus, driven by an 8-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate (bytes/sec) across the bus that this microprocessor can sustain? To increase its performance, would it be better to make its external data bus 32 bits or to double the external clock frequency supplied to the microprocessor? State any other assumptions you make and explain.

Hint: Determine the number of bytes that can be transferred per bus cycle.

E. Consider two microprocessors having 8- and 16-bit-wide external data buses, respectively. The two processors are identical otherwise and their bus cycles take just as long.

- **a.** Suppose all instructions and operands are two bytes long. By what factor do the maximum data transfer rates differ?
- **b.** Repeat if half of the operands and instructions are one-byte long.

F. The Intel 8086 is a 16-bit processor similar in many ways to the 8-bit 8088. The 8086 uses a 16-bit bus that can transfer 2 bytes at a time, provided that the

lower-order byte has an even address. However, the 8086 allows both even- and odd-aligned word operands. If an odd-aligned word is referenced, two memory cycles, each consisting of four bus cycles, are required to transfer the word. Consider an instruction on the 8086 that involves two 16-bit operands. How long does it take to fetch the operands? Give the range of possible answers. Assume a clocking rate of 4 MHz and no wait states.

G. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 32 bits long, 40% are 16 bits long, and 40% are only 8 bits long. Calculate the improvement achieved when fetching instructions and operands with the 32-bit microprocessor.

(a) Instruction format

(b) Integer format

Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

Figure 01 Characteristics of a Hypothetical Machine

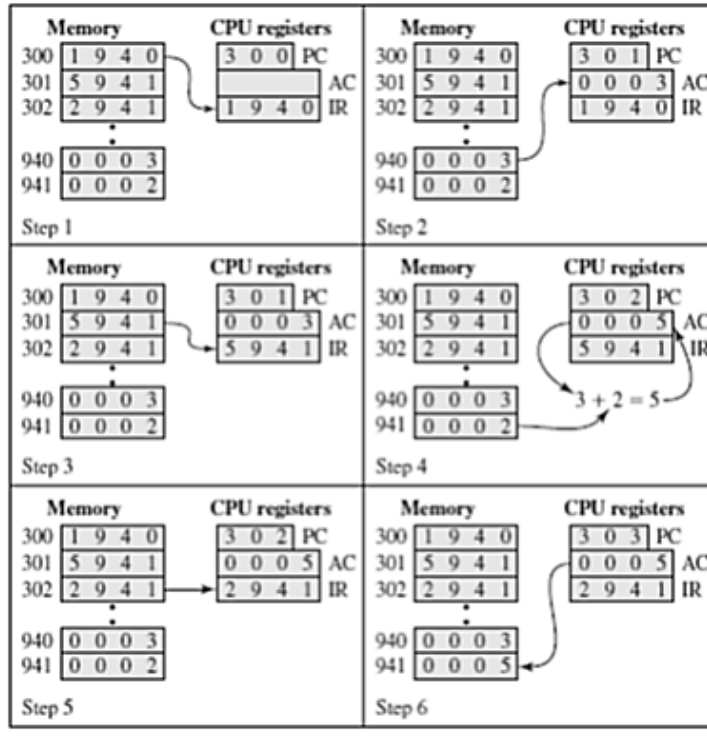

Figure 02 Example of Program Execution (contents of memory and registers in hexadecimal)