



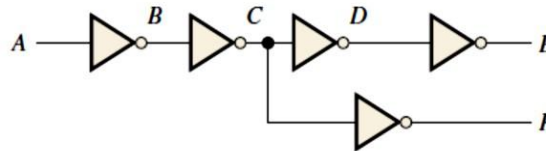
**Program: BC (CS)**  
**Subject: Digital Logic Design (Theory)**  
**Assignment Number: 02**  
**Course Code: CSC-201**  
**EDP Code: 102010016**  
**Semester: Fall 2020**

**Q.1** The input waveform shown in Figure 01 is applied to a system of two inverters connected in a series. Draw the output waveform across each inverter in proper relation to the input.



**FIGURE 01**

**Q.2** A combination of inverters is shown in Figure 02. If a LOW is applied to point A, determine the net output at points E and F.



**FIGURE 02**

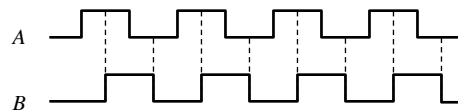
**Q.3** If the waveform in Figure 01 is applied to point A in Figure 02, determine the waveforms at points B through F.

**Q.4** Determine the output, X, for a 2-input AND gate with the input waveforms shown in Figure 03.



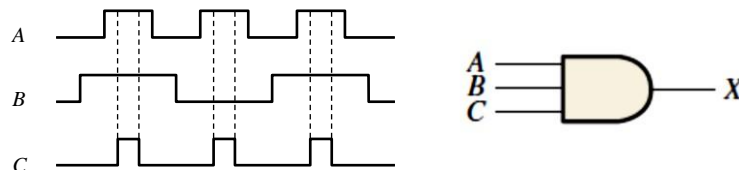
**FIGURE 03**

**Q.5** The waveforms in Figure 04 are applied to points A and B of a 2-input AND gate followed by an inverter. Draw the output waveform.



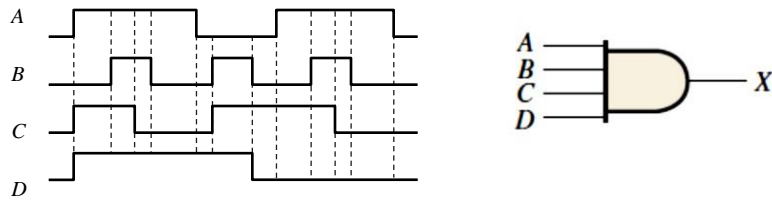
**FIGURE 04**

**Q.6** The input waveforms applied to a 3-input AND gate are as indicated in Figure 05. Show the output waveform in proper relation to the inputs with a timing diagram.



**FIGURE 05**

**Q.7** The input waveforms applied to a 4-input AND gate are as indicated in Figure 06. The output of the AND gate is fed to an inverter. Draw the net output waveform of this system.



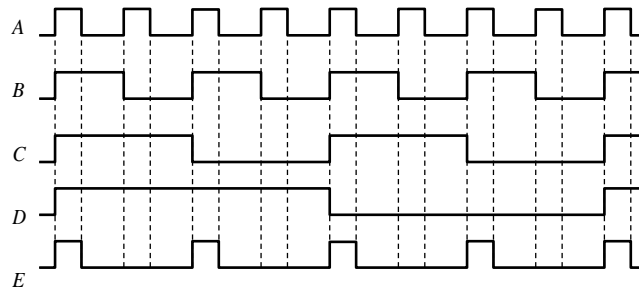
**FIGURE 06**

**Q.8** Determine the output for a 2-input OR gate when the input waveforms are as in Figure 04 and draw a timing diagram.

**Q.9** Repeat Q.6 for a 3-input OR gate.

**Q.10** Repeat Q.7 for a 4-input OR gate.

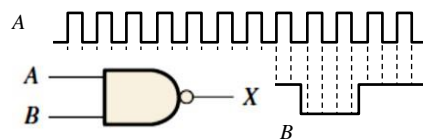
**Q.11** For the waveforms given in Figure 07, A and B are ANDed with output F, D and E are ANDed with output G, and C, F, and G are ORed. Draw the net output waveform.



**FIGURE 07**

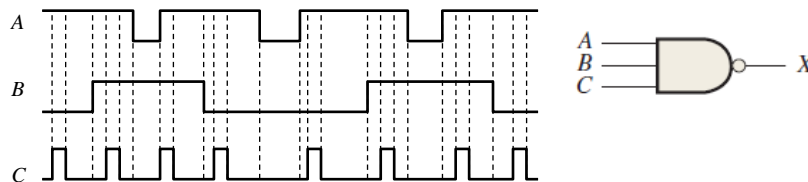
**Q.12** Show the truth table for a system of a 3-input OR gate followed by an inverter.

**Q.13** For the set of input waveforms in Figure 08, determine the output for the gate shown and draw the timing diagram.



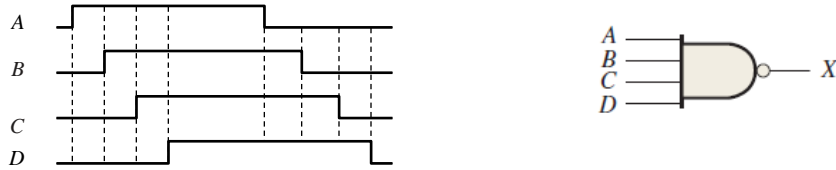
**FIGURE 08**

**Q.14** Determine the gate output for the input waveforms in Figure 09 and draw the timing diagram.



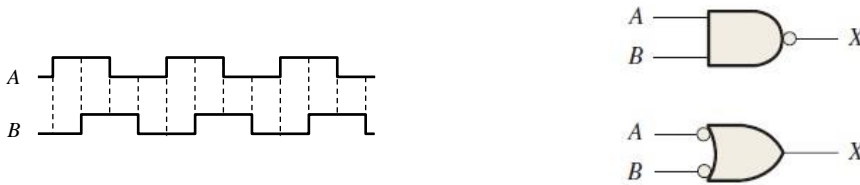
**FIGURE 09**

**Q.15** Determine the output waveform in Figure 10.



**FIGURE 10**

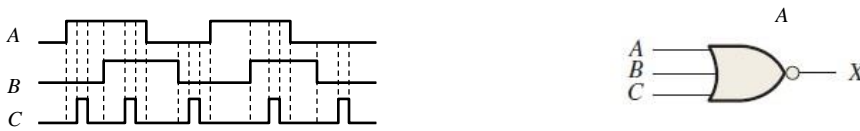
**Q.16** The two logic symbols shown in Figure 11 represent equivalent operations. The difference between the two is strictly from a functional viewpoint. For the NAND symbol, look for two HIGHS on the inputs to give a LOW output. For the negative-OR, look for at least one LOW on the inputs to give a HIGH on the output. Using these two functional viewpoints, show that each gate will produce the same output for the given inputs.



**FIGURE 11**

**Q.17** Repeat Q.13 for a 2-input NOR gate.

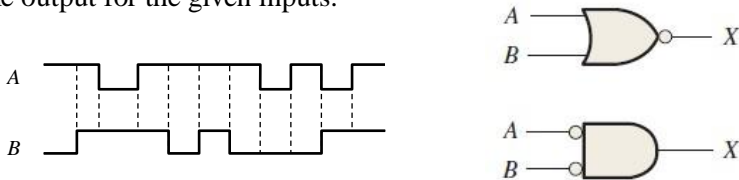
**Q.18** Determine the output waveform in Figure 12 and draw the timing diagram.



**FIGURE 12**

**Q.19** Repeat Q.15 for a 4-input NOR gate.

**Q.20** The NAND and the negative-OR symbols represent equivalent operations, but they are functionally different. For the NOR symbol, look for at least one HIGH on the inputs to give a LOW on the output. For the negative-AND, look for two LOWs on the inputs to give a HIGH output. Using these two functional points of view, show that both gates in Figure 12 will produce the same output for the given inputs.



**FIGURE 13**

**Q.21** Repeat Q.5 for an exclusive-OR gate.

**Q.22** Repeat Q.5 for an exclusive-NOR gate.