Program: BC (CS)

Subject: Computer Architecture

Assignment Number: 01

Course Code: CSC-208

EDP Code: 102010027

Semester: Fall 2020

Q.1 Give answer to each of the following:

A. What are the four main functions of a computer?

B. Figure 01 shows the IBM zEnterprise EC12 Core layout. Briefly explain the function of each sub-area.

C. Discuss the IAS operation using the flowchart in Figure 02.

D. For each of the following examples, determine whether this is an embedded system, explaining why or why not.

   a. Are programs that understand physics and/or hardware embedded? For example, one that uses finite-element methods to predict fluid flow over airplane wings?

   b. Is the internal microprocessor controlling a disk drive an example of an embedded system?

   c. I/O drivers control hardware, so does the presence of an I/O driver imply that the computer executing the driver is embedded?

   d. Is a PDA (Personal Digital Assistant) an embedded system?

   e. Is the microprocessor controlling a cell phone an embedded system?

   f. Are the computers in a big phased-array radar considered embedded? These radars are 10-story buildings with one to three 100-foot diameter radiating patches on the sloped sides of the building.

   g. Is a traditional flight management system (FMS) built into an airplane cockpit considered embedded?

   h. Are the computers in a hardware-in-the-loop (HIL) simulator embedded?

   i. Is the computer controlling a pacemaker in a person's chest an embedded computer?

j. Is the computer controlling fuel injection in an automobile engine embedded?

Q.2 Write a note on each of the following:

A. Main structural components of a computer

B. Key characteristics of a planned computer family

C. Stored program computer

D. Moore's law

Q.3 Differentiate each of the following:

A. Computer organization and computer architecture

B. RISC and CISC

C. Microprocessors and Microcontrollers

D. Cortex-A, Cortex-R, and Cortex-M

Q.4 Solve each of the following:

A. Given the memory contents of the IAS computer shown below,

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB

a. show the assembly language code for the program, starting at address 08A.

b. Explain what this program does.

B. On the IAS, what would the machine code instruction look like to load the contents of memory address 2 to the accumulator? How many trips to memory does the CPU need to make to complete this instruction during the instruction cycle?

C. In Figure 03, indicate the width, in bits, of each data path (e.g., between AC and ALU).

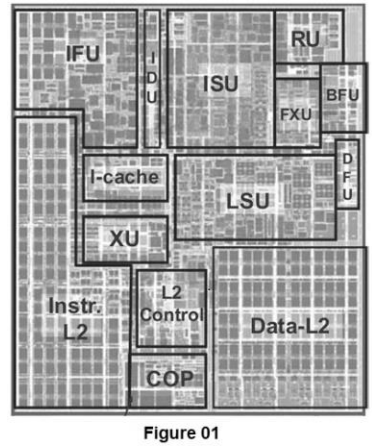

Figure 01

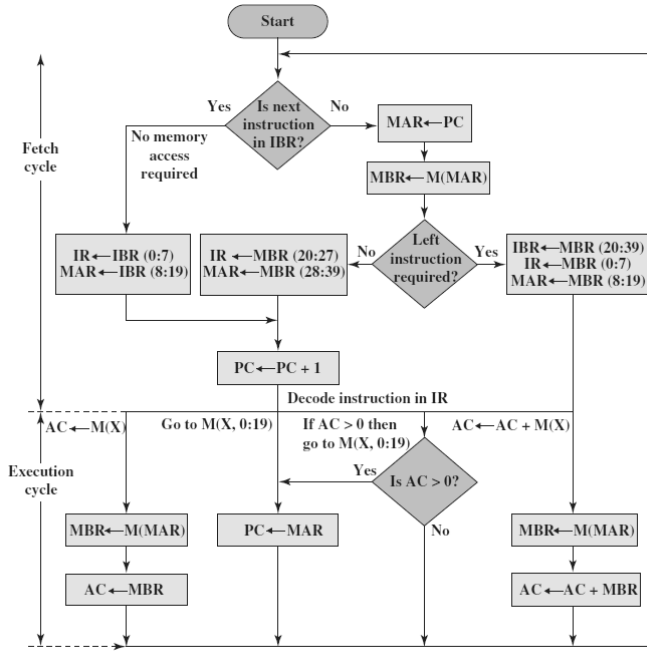
Start
Is next instruction in IBR?
Yes
No
No memory access required
MAR←PC
MBR←M(MAR)
Left instruction required?
No
Yes
IR←IBR (0:7)
MAR←IBR (8:19)
IR←MBR (20:27)
MAR←MBR (28:39)
IBR←MBR (20:39)
IR←MBR (0:7)
MAR←MBR (8:19)
PC←PC + 1
Decode instruction in IR
Fetch cycle
Execution cycle
AC←M(X)
Go to M(X, 0:19)
If AC > 0 then go to M(X, 0:19)
AC←AC + M(X)
Is AC > 0?
Yes
No
MBR←M(MAR)
PC←MAR
MBR←M(MAR)
AC←MBR
AC←AC + MBR

Figure 02

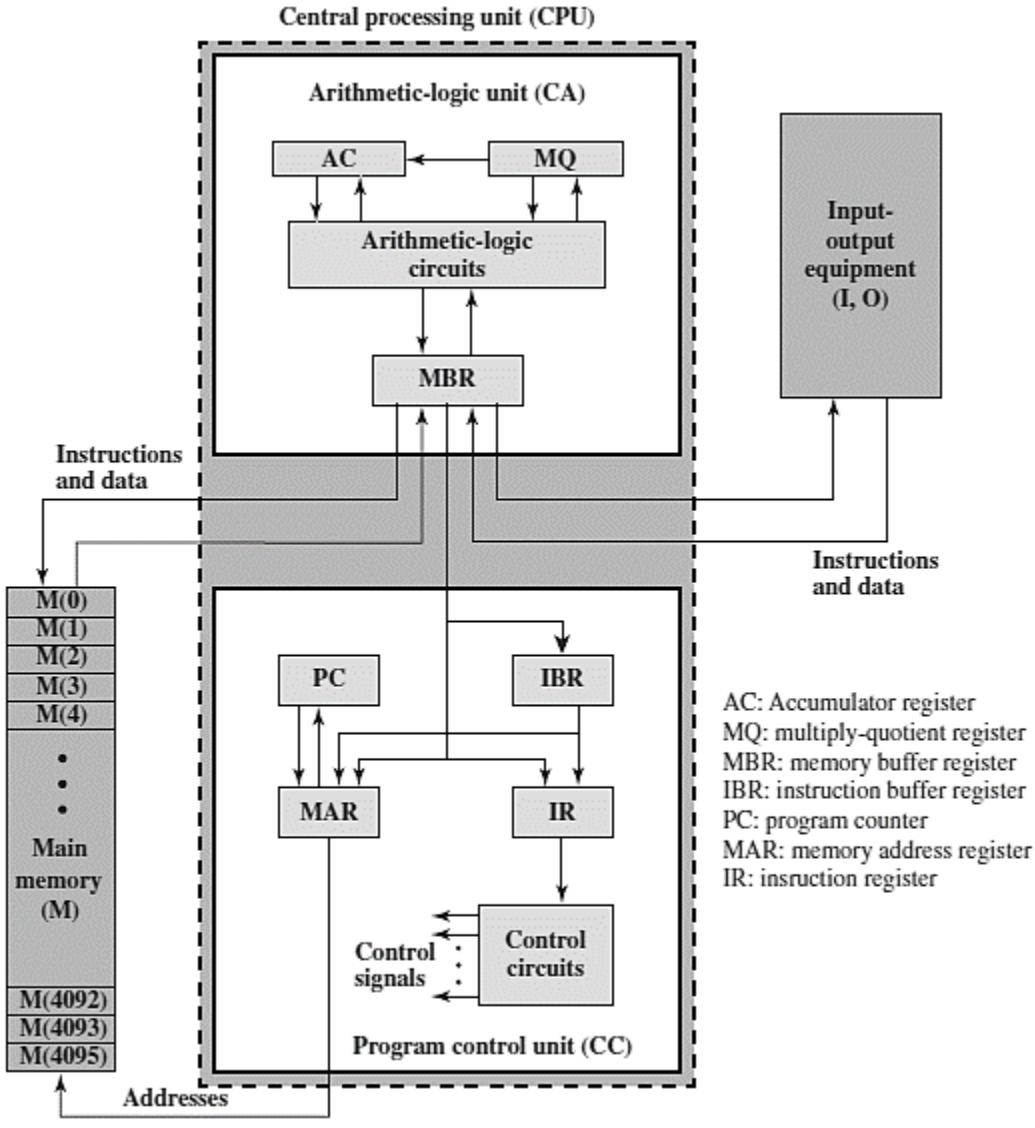

Figure 03 IAS Structure