





PRACTICE PROBLEM 8-2 Using MultiSim, change the supply voltage of Fig. 8-3 to 15 V and measure V_{CE} . Compare your measured value to the answer of Practice Problem 8-1.

8-2 Accurate VDB Analysis

What is a well-designed VDB circuit? It is one in which the voltage divider appears stiff to the input resistance of the base. The meaning of the last sentence needs to be discussed.

Source Resistance

Chapter 1 introduced the idea of a stiff voltage source:

Stiff voltage source: $R_S < 0.01 R_L$

When this condition is satisfied, the load voltage is within 1 percent of the ideal voltage. Now, let us extend this idea to the voltage divider.



What is the Thevenin resistance of the voltage divider in Fig. 8-4*a*? Looking back into the voltage divider with V_{CC} grounded, we see R_1 in parallel with R_2 . As an equation:

$R_{TH} = R_1 ||R_2|$

Because of this resistance, the output voltage of the voltage divider is not ideal. A more accurate analysis includes the Thevenin resistance, as shown in Fig. 8-4b. The current through this Thevenin resistance reduces the base voltage from the ideal value of V_{BB} .

Load Resistance

How much less than ideal is the base voltage? The voltage divider has to supply the base current in Fig. 8-4b. Put another way, the voltage divider sees a load resistance of $R_{\rm IN}$, as shown in Fig. 8-4c. For the voltage divider to appear stiff to the base, the 100 : 1 rule:

$$R_{s} < 0.01 R_{L}$$

translates to:

$R_1 || R_2 < 0.01 R_{\rm IN}$

(8-7)

A well-designed VDB circuit will satisfy this condition.

Stiff Voltage Divider

If the transistor of Fig. 8-4c has a current gain of 100, its collector current is 100 times greater than the base current. This implies that the emitter current is also 100 times greater than the base current. When seen from the base side of the transistor, the emitter resistance R_E appears to be 100 times larger. As a derivation:

$$R_{\rm IN} = \beta_{\rm dc} R_E \tag{8-8}$$

Therefore, Eq. (8-7) may be written as:

Stiff voltage divider:
$$R_1 | R_2 < 0.01 \beta_{dc} R_E$$
 (8-9)

Whenever possible, a designer selects circuit values to satisfy this 100:1 rule because it will produce an ultrastable Q point.

Firm Voltage Divider

Sometimes a stiff design results in such small values of R_1 and R_2 that other problems arise (discussed later). In this case, many designers compromise by using this rule:

Firm voltage divider:
$$R_1 || R_2 \le 0.1 \beta_{de} R_E$$
 (8-10)

We call any voltage divider that satisfies this 10 : 1 rule a **firm voltage divider**. In the worst case, using a firm voltage divider means that the collector current will be approximately 10 percent lower than the stiff value. This is acceptable in many applications because the VDB circuit still has a reasonably stable Q point.

A Closer Approximation

If you want a more accurate value for the emitter current, you can use the following derivation:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + (R_1 || R_2) / \beta_{dc}}$$
(8-11)

This differs from the stiff value because $(R_1||R_2)/\beta_{dc}$ is in the denominator. As this term approaches zero, the equation simplifies to the stiff value.

Equation (8-11) will improve the analysis, but it is a fairly complicated formula. If you have a computer and need a more accurate analysis obtained with the stiff analysis, you should use MultiSim or an equivalent circuit simulator.

Example 8–3



Is the voltage divider of Fig. 8-5 stiff? Calculate the more accurate value of emitter current using Eq. (8-11).

SOLUTION Check to see whether the 100:1 rule has been used:

Stiff voltage divider: $R_1 || R_2 < 0.01 \beta_{dc} R_E$

The Thevenin resistance of the voltage divider is:

$$R_1 \| R_2 = 10 \text{ k}\Omega \| 2.2 \text{ k}\Omega = \frac{(10 \text{ k}\Omega)(2.2 \text{ k}\Omega)}{10 \text{ k}\Omega + 2.2 \text{ k}\Omega} = 1.8 \text{ k}\Omega$$

The input resistance of the base is:

 $\beta_{\rm dc}R_E = (200)(1 \text{ k}\Omega) = 200 \text{ k}\Omega$

and one-hundredth of this is:

 $0.01\beta_{\rm dc}R_E = 2\,{\rm k}\Omega$

Since 1.8 k Ω is less than 2 k Ω , the voltage divider is stiff. With Eq. (8-11), the emitter current is

$$I_E = \frac{1.8 \text{ V} - 0.7 \text{ V}}{1 \text{ k}\Omega + (1.8 \text{ k}\Omega)/200} = \frac{1.1 \text{ V}}{1 \text{ k}\Omega + 9 \Omega} = 1.09 \text{ m/s}$$

This is extremely close to 1.1 mA, the value we get with the simplified analysis.

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The point is this: You don't have to use Eq. (2-11) to calculate emitter current when the voltage divider is stiff. Even when the voltage divider is firm, the use of Eq. (8-11) will improve the calculation for emitter current only by at most 10 percent. Unless otherwise indicated, from now on all analysis of VDB circuits will use the simplified method.

8-3 VDB Load Line and Q Point

Because of the stiff voltage divider in Fig. 8-6, the emitter voltage is held constant at 1.1 V in the following discussion.

The Q Point

The Q point was calculated in Sec. 8-1. It has a collector current of 1.1 mA and a collector-emitter voltage of 4.94 V. These values are plotted to get the Q point shown in Fig. 8-6. Since voltage-divider bias is derived from emitter bias, the Q point is virtually immune to changes in current gain. One way to move the Q point in Fig. 8-6 is by varying the emitter resistor.

For instance, if the emitter resistance is changed to $2.2 \text{ k}\Omega$, the collector current decreases to:

$$I_E = \frac{1.1 \text{ V}}{2.2 \text{ k}\Omega} = 0.5 \text{ mA}$$

The voltages change as follows:

$$V_C = 10 \text{ V} - (0.5 \text{ mA})(3.6 \text{ k}\Omega) = 8.2 \text{ V}$$

and

 $V_{CE} = 8.2 \text{ V} - 1.1 \text{ V} = 7.1 \text{ V}$

Therefore, the new Q point will be Q_L and will have coordinates of 0.5 mA and 7.1 V.

On the other hand, if we decrease the emitter resistance to 510 Ω , the emitter current increases to:

$$I_E = \frac{1.1 \text{ V}}{510 \Omega} = 2.15 \text{ mA}$$



