Lab 14: Synchronous Counter

14.1 Aim:

Realization of 3-bit synchronous counter design.

14.2 Apparatus Required:

IC 7408, IC 7476, IC 7400, IC 7432 etc.

14.3 Procedure:

- Connections are made as per circuit diagram.
- Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.
- Verify the Truth table .

14.4 Counter Circuit

14.5 Synchronous BCD Counter

The 74 x 160 is a high-speed synchronous decade counter with option for applications in programmable loading / dividers array. Install the 74 x 160 in the place where you had the 74 x 93 and connect pins 1, 3, 4, 5, 6, 7, 9 and 10 to switches and the outputs to the decoder, verify load clear & enable input condition from data sheets.

- Derive the functional table of the 74 x 160, and verify it experimentally.
- Arrange the 74 x 160 as a decade counter.
- Design the 74 x 160 as a divided by 8 using only a single INV gate.

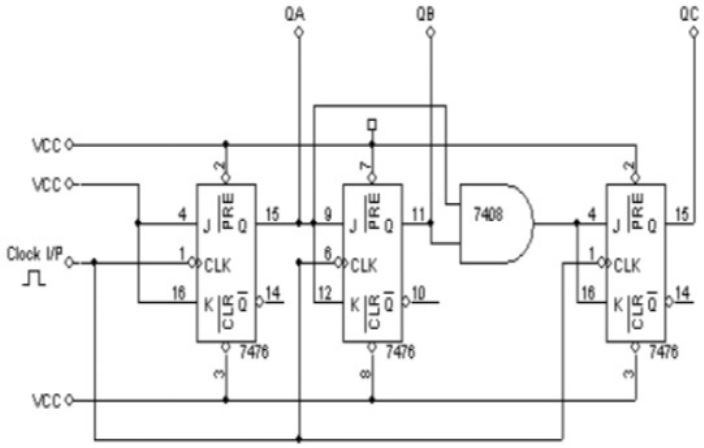

Figure 14.1: 3-bit synchronous counter circuit

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Figure 14.2: 3-bit synchronous counter truth table

- Design the 74 x 160 as a divided by 6 and program the counter to have the sequence 1,2,3,4,5,6,1,2,3,âĂę.. use only a single NAND gate.

14.5.1 Synchronous BCD Up/Down Counter

The 74x190 is a decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 74x190 to be used in programmable dividers. In addition the 74x190 features up/down (u/d) counter operation.

- Derive the functional table for the 74x190 and verify it experimentally.
- Arrange the 74x190 as a decade up, and then down counter.

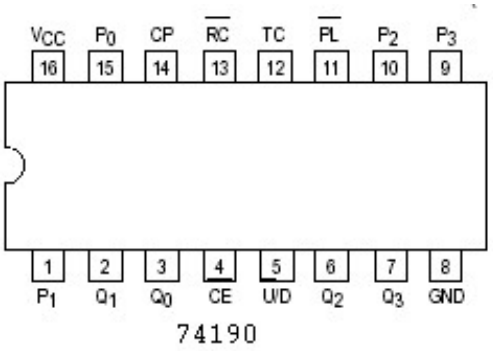

Figure 14.3: Synchronous BCD counter 74160 IC pin specification

- Design the 74x190 as a divided by 7 down counter having the sequence 7,6,5,4,3,2,1,7,6,5, use only a 74x32.
- Design the 74x190 as a divided by 6 up counter having the sequence 3,4,5,6,7,8,3,4,5,6, use only a single NAND gate.

Note: Show schematic diagram for each circuit connections in each part.

14.6 Summary