Department of Electrical Engineering
Assignment
Date: 14/04/2020

Course Details

Course Title: Electronic Circuit Design 2 **Module:** 04
Instructor: Engineer Mujtaba Ehsan **Total Marks:** 30

Student Details

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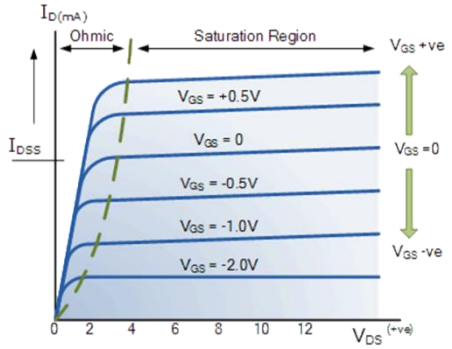
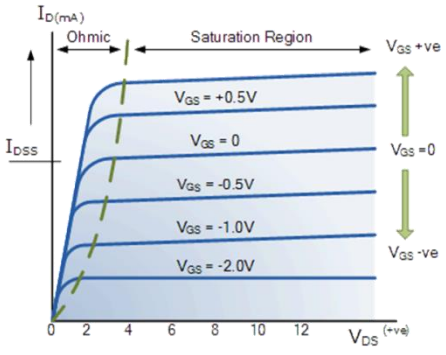
Q1.	(a)	**Explain** the drain characteristic curve of D-MOSFET given below. 	Marks 07 CLO 1
	(b)	**Sketch** the hybrid model and write equations for the transistor in common emitter configuration.	Marks 06 CLO 1
Q2.		A certain operational amplifier has a common mode gain of 0.6 and an open loop differential voltage gain of 400,000. **Evaluate** the CMRR & express it in decibels.	Marks 05 CLO 2
Q3.	(a)	**Explain** the concept behind negative feedback in operational amplifiers.	Marks 06 CLO 2
	(b)	**State** the following statement as **True** or **False** and also give the reason for your answer: "The output of a summing amplifier is positive"	Marks 06 CLO 2

QUESTION NO 1(a):

Explain the drain characteristic curve of D-MOSFET given below.



ANSWER:

Drain characteristics:

Drain characteristics are the characteristics between the Drain current (I_D) and the Voltage V_{DS} for various voltage V_{GS}. Where I_D is the output current V_{DS} Is the output voltage while V_{GS} is the input voltage.

IN CASE OF V_{GS} = 0 V:

As we can see in the above graph when V_{DS} is 0 V the I_D is also 0 A, this is because when V_{DS}=0 then $V_D - V_S$ =0V or we can write V_D=V_S. This means that the potential at drain is same as the potential at source which means there's no potential difference and as there is no potential difference the current I_D will not flow through the channel and will be equal to 0 A. And when we increase the V_{DS} the potential difference will increase and the drain current I_D will also increase linearly but after some time the drain current I_D becomes constant and the reason is pinch-off at V_{GS}=0 V. When V_{GS}=0 V it gives us the saturated drain current we call it I_{DSS}.

In case of D-MOSFET(depletion type MOSFET) we can either increase or decrease the value of V_{GS} i.e +0.5 V, -0.5V, -1 V and -2 V etc, to gain curves at different points and this is the plus point of D-MOSFET while in JEFT we cannot make the V_{GS} positive we can only make it negative.

IN CASE OF POSITIVE V_{GS} OR V_{GS} = +0.5V:

In case of V_{GS}= +0.5V the gate terminal becomes positive and as gate terminal becomes positive the free charge carrier in the p-type substrate which are electron will be attracted towards the gate and the channel will now have more electrons. And as the number of electrons increases definitely the current will also increase. So, for same V_{DS} the drain current I_D will be larger when V_{GS} is +0.5 V. And on increasing V_{DS} the drain current I_D will increase linearly and after some time

will become constant due to pinch off. As we can see the gape between the lines when V_{GS} =0 and when V_{GS} =+0.5, it shows that if we make the V_{GS} to +0.5 the drain current I_D increases rapidly.

IN CASE OF NEGATIVE V_{GS} OR V_{GS} = -0.5V:

In case of V_{GS}= -0.5V the gate terminal becomes negative and as gate terminal becomes negative the free charge carrier electrons in the N-channel will be pushed down and the holes in the p-type substrate will be attracted towards the gate and due to this electrons will recombine with the holes and the number of free electron for conduction in N-channel reduces and this will also reduce the drain current I_D when we make V_{GS} =-0.5 V. The current will increase linearly and after some time will become constant due to pinch off. So, for same V_{DS} the drain current I_D will be smaller when V_{DS}=-0.5 V. As we can see the gap between the lines when V_{GS} =0 and when V_{GS} =-0.5, it shows that if we make the V_{GS} to -0.5 the drain current I_D will decrease rapidly.

Same procedure will happen if decrease the V_{GS} to -1 V and -2 V.

QUESTION NO 1(B)

Sketch the hybrid model and write equations for the transistor in common emitter configuration.

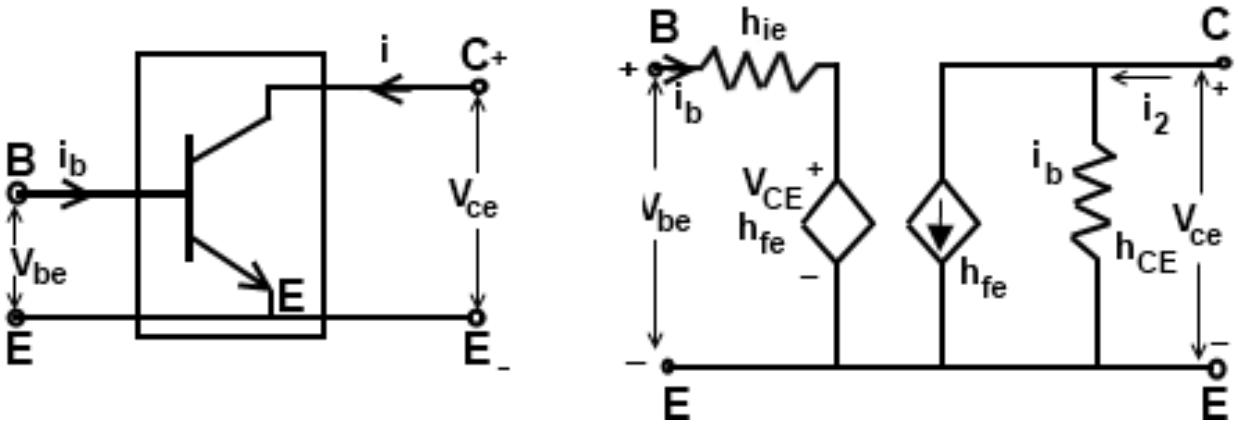
ANSWER:

In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and emitter terminals. The input voltage (V_{be}) and the output current (i_e) are given by the following equations:

$V_{be} = h_{ie}.i_b + h_{re}.V_c$

$i_e = h_{fe}.i_b + h_{oe}.V_c$

CIRCUIT DIAGRAM:



COMMON EMITTER CONFIGURATION:

Where $h_{ie} = (\partial f_1/\partial i_B)V_c = (\partial v_B/\partial i_B)V_c = (\Delta v_B/\Delta i_B)V_c = (v_b / i_b)V_c$

$h_{re} = (\partial f_1/\partial v_c)I_B = (\partial v_B/\partial v_c)\, I_B = (\Delta v_B/\Delta v_c)\, I_B = (v_b/v_c)\, I_B$

$h_{fe} = (\partial f_2/\partial i_B)V_c = (\partial i_c/\partial i_B)V_c = (\Delta i_c/\Delta i_B)V_c = (i_c / i_b)V_c$

$h_{oe} = (\partial f_2/\partial v_c)I_B = (\partial i_c/\partial v_c)\, I_B = (\Delta i_c/\Delta v_c)\, I_B = (i_c/v_c)\, I_B$

QUESTION NO: 2

A certain operational amplifier has a common mode gain of 0.6 and an open loop differential voltage gain of 400,000. **Evaluate** the CMRR & express it in decibels.

Given:

Aol= Open Loop differential voltage gain= 400,000

Acm= Common mode gain= 0.6

Required:

CMRR=?

Solution:

Formula:

As CMRR= Aol/Acm

Therefore

CMRR= 400,000/0.6

= 666,666.667

CMRR in decibels:

Formula :

CMRR= 20 log(Aol/ Acm)

= 20 log (666,666.667)

=116.478Db Answer.

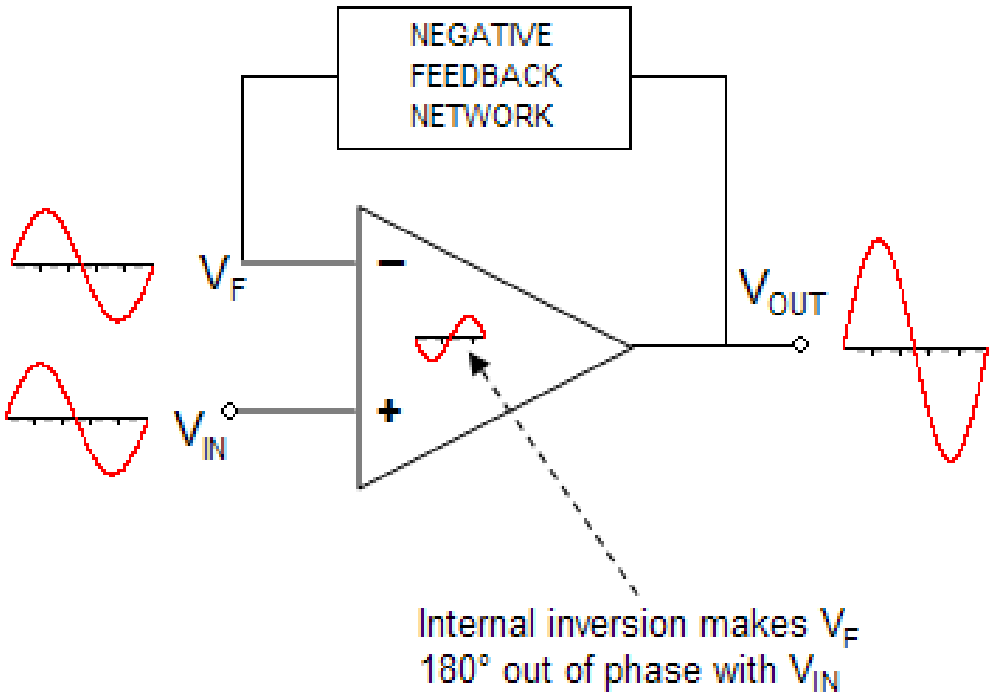
QUESTION NO: 3(a)

Explain the concept behind negative feedback in operational amplifiers.

ANSWER:

"**Negative feedback** is the process whereby a portion of the output voltage of an amplifier is returned to the input with a phase angle that opposes (or subtracts from) the input signal"

Inverting (-) input effectively makes the feedback signal 180' out of phase with the input signal.



An ideal op-amp has infinite gain. It amplifies the difference in voltage between the + and - pins. Of course, in reality this gain is not infinite, but still quite large.

The output of the op-amp (at to some extents the input also) is constrained by the power supply, we can't get out more than the supply puts in.

If we simply put signals into the op-amp without feedback it would multiply them by infinity and get a binary output (it would saturate at the supply rails)

So, we need some way of controlling the gain. That is what the feedback does.

The feedback (DC as well as AC) takes part of the amplified output from the input, such that the gain is constrained much more by the feedback network, which is predictable, and much less by the massive (and unpredictable) open loop gain.

Even in an AC only circuit we still need feedback that works at DC (zero Hz) or the gain would be only that of the open loop for DC signals. You AC signal though constrained would be swamped by the DC open loop gain.

Negative feedback stabilizes the op-amp by reducing its gain. In open loop, it has theoretically infinite gain, and thus if only a small voltage is applied at the input, the output will saturate in the direction of one of the supply voltages (Vcc or Vss). V+=input V-=Vout/2, If we have a gain of 2, it's obvious that V+ is Vout/2.

Negative feedback results in reduced overall voltage gain, a number of improvements are obtained, among them being:

1. Higher input impedance.

2. Better stabilized voltage gain.

3. Improved frequency response.

4. Lower output impedance.

5. Reduced noise.

6. More linear operation.

QUESTION NO: 3(b)

State the following statement as **True** or **False** and also give the reason for your answer:
"The output of a summing amplifier is positive".

ANSWER:

The above statement is ''False''. Following is the reason.

To calculate the formula of a summing amplifier we have a formula which is,

$$V_{OUT} = -R_F \left[\frac{V1}{R1} + \frac{V2}{R2} + \frac{V3}{R3}\right]$$

As we can see in the above equation it'll give us a positive output if the sum of input voltage divided by input resistance (R_{in}) is equal to a negative number, while if the resultant from input voltages divided by input resistance (R_{in}) is a positive number then our V_{out} will be a negative value.

Summing amplifier is an application of inverting op-amp configuration that has two or more inputs and its output voltage is proportional to the negative of the algebraic sum of its input voltages."

For Example:

A:

V1= 2V , R1=5 KΩ

V2=3V , R2=5 KΩ

V3=5V , R3=5 KΩ

R_F =5 KΩ

Putting the values in the above equation we get,

$$V_{OUT} = -5\ \text{KΩ}\ \left[\frac{2V}{5\ \text{KΩ}} + \frac{3V}{5\ \text{KΩ}} + \frac{5V}{5\ \text{KΩ}}\right]$$

$V_{OUT} = -10V$ Answer.

B:

V1= - 2V , R1=200 KΩ

V2=3V , R2=500 KΩ

V3=1V , R3=1 MΩ

R_F =1 MΩ

$$V_{OUT} = -1000\ \text{KΩ}\ \left[\frac{-2V}{200\ \text{KΩ}} + \frac{3V}{500\ \text{KΩ}} + \frac{1V}{1000\text{KΩ}}\right]$$

$V_{OUT} = +3V$ Answer.
