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Assignment # 3.

Q1
A)
Ans:-

The first is to disable interrupts while an interrupt is being processed A disabled interrupt simply means that the processor can & will ignore the interrupt request signal.

The drawback to the preceding approach is that it does not take into account relative priority or time critical needs.

2) A second approach is to define priorities for interrupts & to allow an interrupt of higher priority to causes a lower-priority interrupt handler to be itself interrupted.

B)
Ans:-

Q P1 Protocal Layer:- In this layer the packet is defined as the unit of transfer. One key function performed at this level is a Cache Coherency

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Protocal which deals with making sure that main memory value held in multiple caches are consistent A typical data packets payload is a block of data being sent to or from a cache

C>
And:-

Physical & logical Architecture od PCIe:-

A Root Complex- device also reffered to as a chipset or a host bridge Connects the processor & memory subsystem to the PCI Express switch fabric comprising one or more PCIs & PCIe switch devices.

PCIe link from the chipset may attach to the following kinds of devices that implement PCIs.
Switch: The switch manges multiple PCIs streams.

Q2
A)
And:-

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PCIe endpoint:
An I/o devices core controller that implements PCIe such as a 1Gigabit ethernet switch a graphics or video controller, disk interface, or a communication controller.

Legacy endpoint:-
Legacy endpoint is intended for existing designs that have been migrated to PCI Express, & it allows legacy behavior such as use of I/o space & locked transactions.

PCIe/PCI bridges:-
Allow older PCI devices to be connected to PCI-based system.

Q2
A)
Ans:-
Instruction cycle:-
The Processing required for a single instruction is called an instruction cycle. Using the simplified two step description given previously, the

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Instruction cycle is depicted. The two step are refferred to as the fetch cycle & the execute cycle. Program execution halts only if the machine is turned off. Some sort of unrecoverable error occure or a program instruction that halts the computer is encountered.

B)
Ans:

Class of Interrupts:-

Program:

It is generated by some condition that occured as a result of an instruction execution such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a User's allowed memory space.

Timer:

It is generated by Timer within the processor. this allows the operating system to perform certain functions on a regular basis.

I/O:

It is generated by I/O

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It is generated by I/O Controller to signal normal completion of an operation request service from the processor or to signal a variety of error condition.

Hardware failures:-
It is generated by failure such as power failure or memory parity error.

c)
Ans:-
Interconnection Schemes:-
The most common computer interconnection structure are based on the use of one or more system buses.
A system bus typically of from about fifty to hundered of seperate line.

Data lines:-
The data line prowide a path for moving data among system modules. These line collectively are called the data bus.

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Address lines:

The address lines are used to designate the source or destination of the data on the data bus.

Control lines:

The control line are used to control the access to and the used of the data & address line.

Q3 (A)

Ans

Programming hardware:

The program is the form of hardware and is termed a hardware program.

Programming in software:

The new method of the programming which is a sequence of code or instruction is called Software programming.

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B)
Ans:-

In the interrupt cycle, the Processor checks to see if any interrupts have occurred indicated by the Presence of an interrupt signal.

If no interrupts are pending the processor proceeds to the fetch cycle & fetch the next instruction of the current Program.

Q4
A)

The hypothetical machine of has two (I/o instruction).
0011 = Load AC form I/O
0111 = Store AC to I/O

Load AC to device 5
Store AC to device 6.

B)
Ans:-

The Pc Contain 300 the address of the first instruction.

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The value in location 940 is loaded in the MBR.

The address portion of the IR(940) is loaded to MBR.

The value in the PC (301) is loaded to the MAR.

C)

Ans:

a) If the local address bus is 32 bits, the whole address can be transferred at once & decode memory.

b) 2^{24} = 16 MBytes.

c) The Program Counter must be at least 24 bits Typically a 32-bits microprocessor with have a 32-bit external address.

D)

Ans:-

Clock cycle =
1 = 125ns 8 MHz Bus cycle = 4×125ns
= 500ns 2 bytes transferred every 500ns

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4 MB/sec:

Doubling the frequency may mean adopting a new chip manufacturing technology doubling the external instruction will have the same number of clock cycle.

E)

Ans:

a) During a single bus cycle the 8-bits microprocessor transfer one byte while the 16-bits microprocessor transfer two bytes.

b)

Suppose we do 100 transfer of operands & instruction of which 50 are one byte long & 50 are two byte long.

F)

Ans:

A bus cycle take 0.25 μs so a memory cycle takes 1 μs. If both operand are even aligned, it take 2 μs to fetch the two operands.

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6)
Ans:-

Consider a min of 100 instruction & operand. on average they consist of 20% 32 bit item, 40% 16 bit item, & 40% 8 bit items. the number of bus cycle required for the 16 bit microprocessor $(2 \times 20) + 40 + 40 = 120$ for the 32 bit microprocessor the number required is 100 this amount an improvement of 20/120 or about 17%