

Assignment NO : 2

Name : Asad Khan

ID : 14944

Subject : Computer Architecture

Submit To : Sir M. Amin

Department : BS(CS)

Semester. 4th

Question No: 1
Give Answer each of the following.

Question No: 1(A)

Ans

Different desktop applications that require the great power of contemporary microprocessor based system are:

- ✓ Image processing
- ✓ Three-dimensional rendering
- ✓ Speech recognition
- ✓ Videoconferencing
- ✓ Multimedia authoring
- ✓ Voice and video annotation of files
- ✓ Simulation modelling

Question No. 1(B)

Answer

The Techniques used in contemporary processors to increase speed are following:

Pipelining:

pipelining enables a processor to

Name: Asad Khan
ID: 14944
Page: 02

work simultaneously on multiple instructions by performing a different phase for each of the multiple instruction of at the same time.

* Branch prediction:

Branch prediction potentially increases the amount of work available for the processor to execute.

* Superscalar execution:

This is the ability to issue more than one instruction in every processor clock cycle. In effect, multiple parallel pipelines are used.

* Data flow analysis:

The processor analyzes which instructions are dependent on each other's results, or data, to create an optimized schedule of instructions.

* Speculative execution:

This enables the processor to keep its execution engines

as busy as possible by executing instructions that are likely to be needed.

Question No: 1(C)

Answer:-

Discuss the problem created due to increases in clock speed and logic density of the processor are:-

• Power:

As the density of the logic and the clock speed on a chip increases so the power density increases and also dissipated the heat.

• RC delay:-

The speed at which electrons can flow on a chip between transistors is limited by the resistance and capacitance of the metal wires connecting them, specifically, delay increases as the RC product increases.

• Memory latency:-

Memory access speed (latency)

and Transfer speed (Throughput) by processor speeds.

Question No: 1 (D)

Answer:

The speedup using a parallel processor with N processors that fully exploits the parallel portion of the program is as follows:-

speedup = Time to execute program on a single processor / Time to execute program on N parallel processors.

$$= T(1-f) + Tf / T(1-f) + Tf/N = 1 / (1-f) + f/N$$

Question No: 1 (E)

Answer:

Multicore:

* The use of Multiple processors on the same chip provides the potential to increase performance without increasing the clock rate.

* Strategy is to use two simpler

Name: Asad Khan
ID :: 14944
Page No 05

- ▶ Processors on the chip rather than one more complex processor.
- ▶ With two processors larger caches are justified.
- ▶ As caches became larger it made performance sense to create two and then three levels of cache on a chip. MIC:
- ▶ Keep in performance as well as the challenges in developing software to exploit such a large number of cores.
- ▶ The multicore and MIC strategy involves a homogeneous collection of general purpose processors on a single chip.
Gpus.
- ▶ Core designed to perform parallel operations on graphics data.
Traditionally found on a plug-in graphics card, it is used to encode and render 2D and 3D graphics as well

Name: Asad Khan
ID: 14944
Page: 06

as process video.
used as vector processors for a variety of applications that require repetitive computations.

Question No: 2

Solve each of the following.
2(A)

Answer:-

Effective CPI:

$$CPI = (1 \cdot 46000) + (2 \cdot 33000) + (2 \cdot 916000) + (2 \cdot 9000) / 100$$

$$CPI = 162000 / 100$$

$$CPI = 1620$$

MIPS Rate:

$$MIPS \text{ rate} = 60 \text{ MHz} / 1620 \cdot 10^6$$

$$MIPS \text{ rate} = 60 \cdot 10^6 / 1620 \cdot 10^6$$

$$MIPS \text{ rate} = 60 / 1620$$

$$MIPS \text{ rate} = 0.037$$

Asad Khan
14944
Page: 06

Name: Asad Khan
ID : 14944
Page: 07

Execution Time:

$$T = IC / (MIPS \cdot 10^6)$$

$$T = 104000 / (0.037 \cdot 10^6)$$

$$T = 104000 / 37 \cdot 10^3$$

$$T = 2811 \cdot 10^{-3}$$

$$T = 2811 \cdot 10^{-3}$$

$$T = 2.811 \text{ sec}$$

Question NO : 2 (B)

Answer:-

For Machine A:

$$CPI = (1 \cdot 8 + 3 \cdot 4 + 4 \cdot 2 + 3 \cdot 4) \cdot 10^6 / (8 + 4 + 2 + 4) \cdot 10^6$$

$$CPI = 40 \cdot 10^6 / 18 \cdot 10^6$$

$$CPI = 2.22$$

$$MIPS \text{ rate} = 200 \text{ MHz} / 2.22 \cdot 10^6$$

$$MIPS \text{ rate} = 200 \cdot 10^6 / 2.22 \cdot 10^6$$

$$MIPS \text{ rate} = 90$$

$$T = IC / (MIPS \cdot 10^6)$$

$$T = 18 \cdot 10^6 / 90 \cdot 10^6$$

$$T = 0.2 \text{ sec}$$

Name Asad Khan
ID 14944
Page 08

For Machine B:

$$CPI = \frac{(1 \cdot 10 + 2 \cdot 8 + 4 \cdot 2 + 3 \cdot 4) \cdot 10^6}{(10 + 8 + 2 + 4) \cdot 10^6}$$

$$CPI = 46/24$$

$$CPI = 1.92$$

$$MIPS \text{ rate} = 200 \text{ MHz} / 1.92 \cdot 10^6$$

$$MIPS \text{ rate} = 200 \cdot 10^6 / 1.92 \cdot 10^6$$

$$MIPS \text{ rate} = 104$$

$$T = IC / (MIPS \cdot 10^6)$$

$$T = 24 \cdot 10^6 / 104 \cdot 10^6$$

$$T = 0.23 \text{ sec}$$

Question NO: 2(C)

(La)

Answer

The MIPS rate could be computed as the following:

$$MIPS \text{ rate} = IC / T \cdot 10^6$$

$$IC = MIPS \text{ rate} \cdot T \cdot 10^6$$

Now by computing the ratio of

Name : Asad Khan
ID : 14944
Page : 09

The instruction count of the IBM RS/6000 to the VAX 11/780 which is

$$18^{\circ} 1 \times 10^6 / 1^{\circ} 12 \times 10^6$$

$$= 18/12$$

$$= 1.5$$

Question No: 2

C(b)

Answer

Regarding to the VAX 11/780, The

$$CPI = (5 \text{ MHz}) / (1^{\circ} 10^6) = 5^{\circ} (10^6 / 1^{\circ} 10^6)$$

$$= 5/1 = 5$$

Regarding to the IBM RS/6000, The

$$CPI = (25 \text{ MHz}) / (18^{\circ} 10^6) = 25^{\circ} 10^6 / 18^{\circ} 10^6$$

$$= 25/18 = 1.4$$

Question NO: 2 (D)

Answer

a - Determine The Average CPI.

Answer

Since we have the same instruction mix, that means the additional instruction for each task

Name : Asad Khan
ID : 14944
Page : 108

could be allocated appropriately between the instruction types. Therefore, the following tables be given.

Instruction Type	CPI	Instruction Mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	12	10%

The average CPI = $(1 \times 0.6) + (2 \times 0.18) + (4 \times 0.12) + (12 \times 0.1) = 2.64$. Therefore, the CPI has been increased since the time for memory access is also increased.

b. Determine the corresponding MIPS rate.

MIPS = $400 / 2.64 \approx 152$. There is a

Name : Asad Khan
ID : 14944
Page : 11

corresponding drop in the MIPS rate
C. calculate the speedup factor.

The speedup factor equals to the ratio of the execution times. The execution time is calculated as the following: $T = I_c / (MIPS \cdot 10^6)$.

For the one processor, $T_1 = (2 \cdot 10^6) / (178 \cdot 10^6) = 11 \text{ms}$.

For the 8 processor, each processor execute $1/8$ of the 2 million instructions plus the 2500

$$T_8 = 2 \cdot 10^6 \div 8 + 0.025 \cdot 10^6 / 152 \cdot 10^6$$

$$T_8 = 18 \text{ms}$$

Therefore we have

Speedup = Time to execute program on a single processor / Time to execute program on N parallel processor

$$\text{Speedup} = 11 / 1.8$$

$$\text{Speedup} = 6.11$$

Name : Asad Khan
ID : 14944
page: 12

Question 2 (D)(d)

By depending on the information given, it is not obvious to how to quantify this effect in Amdahl's evaluation.

Therefore, if it is supposed that that fraction of code, which is parallelizable, is $f = 1$, then Amdahl's law decreases to speedup = $N = 8$.

Therefore,

The actual speedup is only about 75% of the theoretical speedup.