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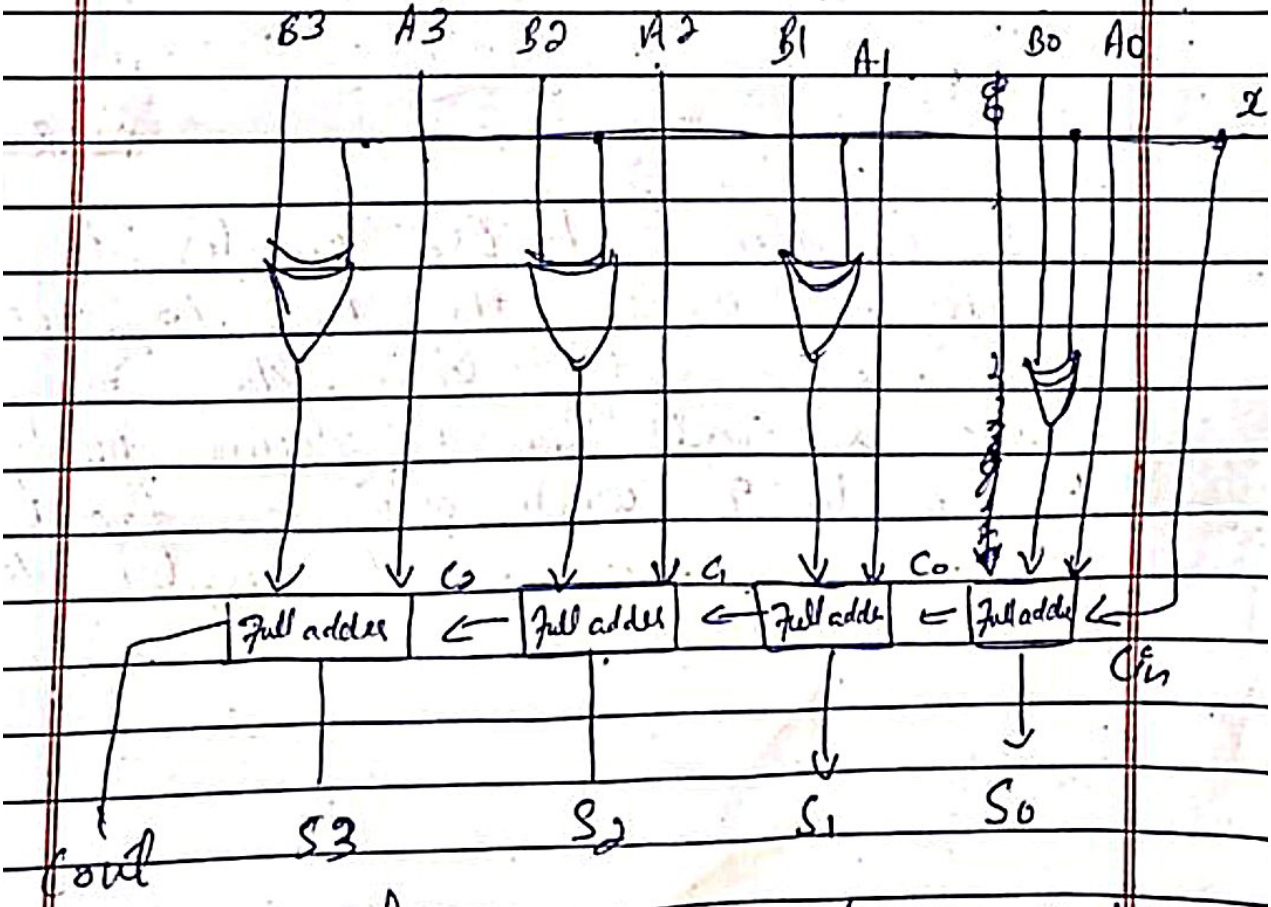
Paper DLD Final Term

Teacher Sir M. Amin

Semester 3rd.

Q/.

Part (a)



In digital circuits A binary Adder-

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Subtracter in one which is capable of both addition and subtractor of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Design) This circuit requires prerequisite knowledge of xor gate, Binary addition and subtraction, full adder.

The circuit consists of 4 full adders since we are performing operations on 4 bit numbers. There is a control line K that holds a binary value of either 0 or 1 which determines that the operation being carried out is addition or subtraction. For an n-bit binary adder-Subtractor we use n number of full adders.

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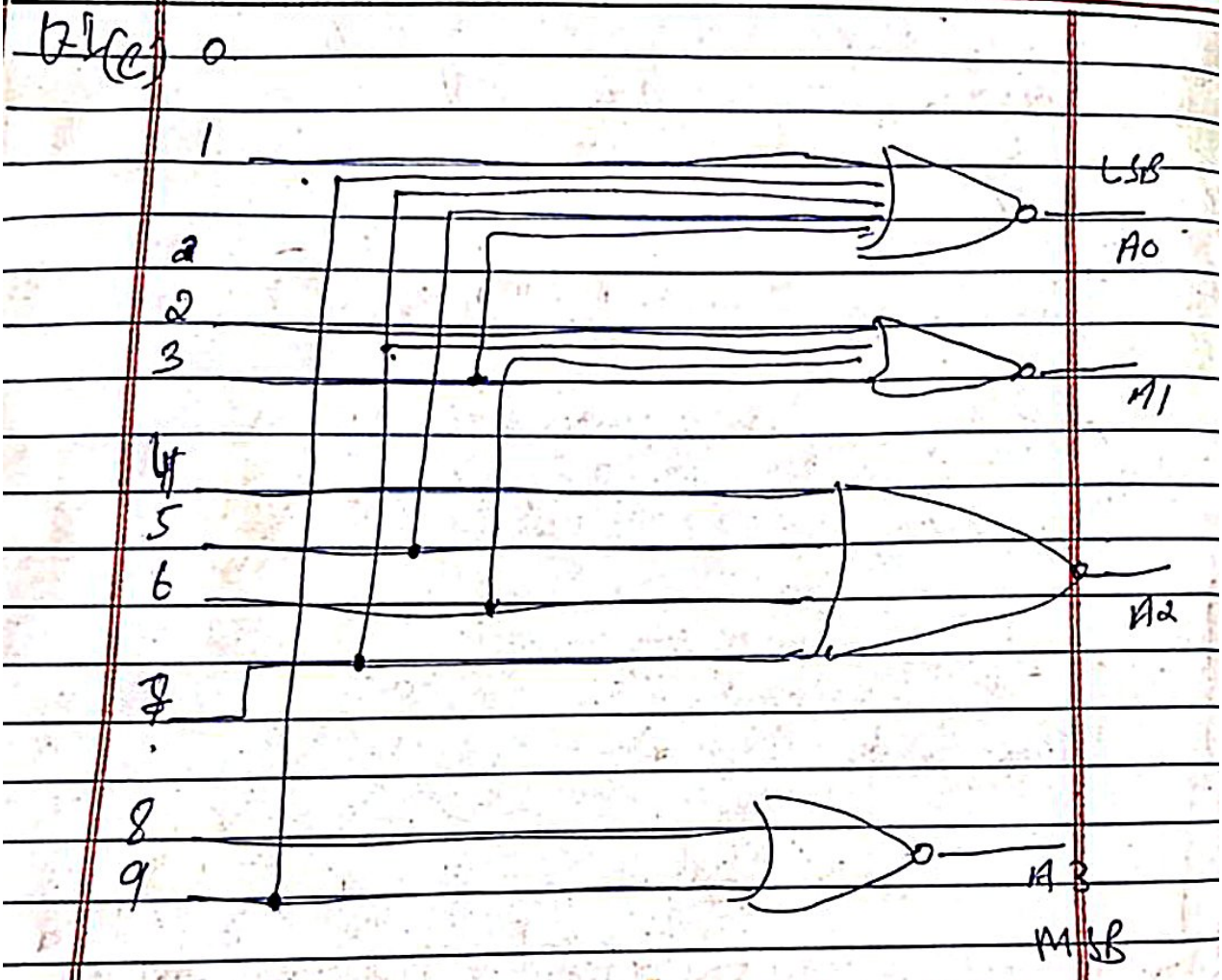

A simple decimal-to-BCD encoder is a digital circuit that has 10 input lines and 4 output lines. The 10 inputs represents the 10 decimal numbers from 0 to 9, where only one input can be active. The output indicates the BCD code that represent the active input

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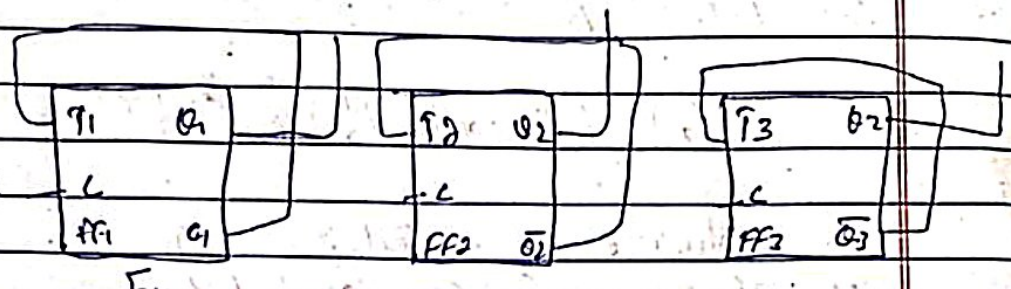
(d) frequency divider (use 3j-k flip flop. and assume 16 kHz. frequency as initial wave form.



Here we assume the fequency is 16 khz

So $f/2 = F = 16/2$

$F = 8$ khz

(b)

input data	here	output
S_1	S_0	Y
0	1	0
1	0	1
1	1	0
0	0	1

If $S_1 = 0$ and $S_0 = 1$ then $y = D_0$

Then $y = D_0 \bar{S_1} (S_0)$

if $S_1 = 1$ and $S_0 = \bar{0}$ then $y = D_1$

Then $y = D_1 (S_1) \bar{S_0}$

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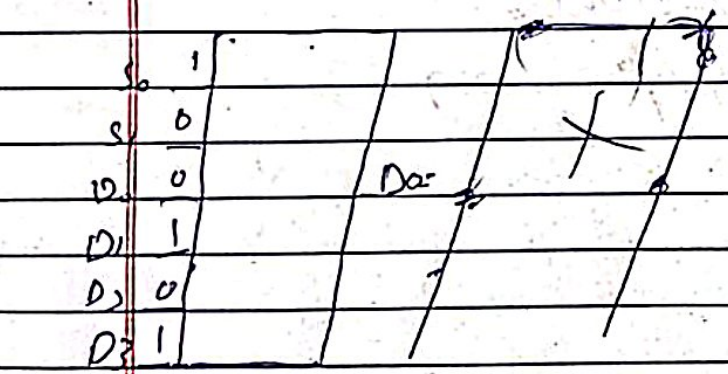
if $S1 = 1$ and $S0 = 1$ then $y = D2$
Then $y = D2 \; S1 (S\bar{0})$

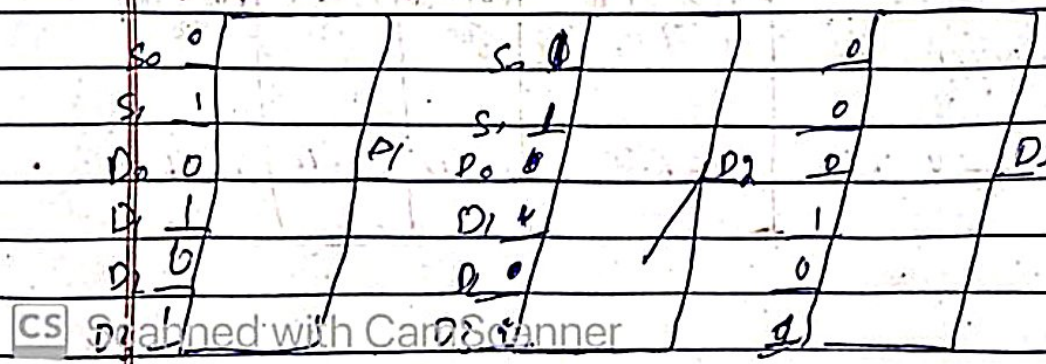
if $S1 = 0$ and $S0 = 1$ then $y = D3$
Then $y = D3 \; S1 \; S0$

$y = D0 (S1)(S0) - D1 (S1) S0 - D2 \; S1 (S0)$
$- D3 \; S1 \; S0$

(A) $S = 1$ $S = 0$



(B) $S0 = 0$, $S1 = 1$ $S_{s=1} \; S1 = 1$ $P = S0 = 0$ $S1 = 0$



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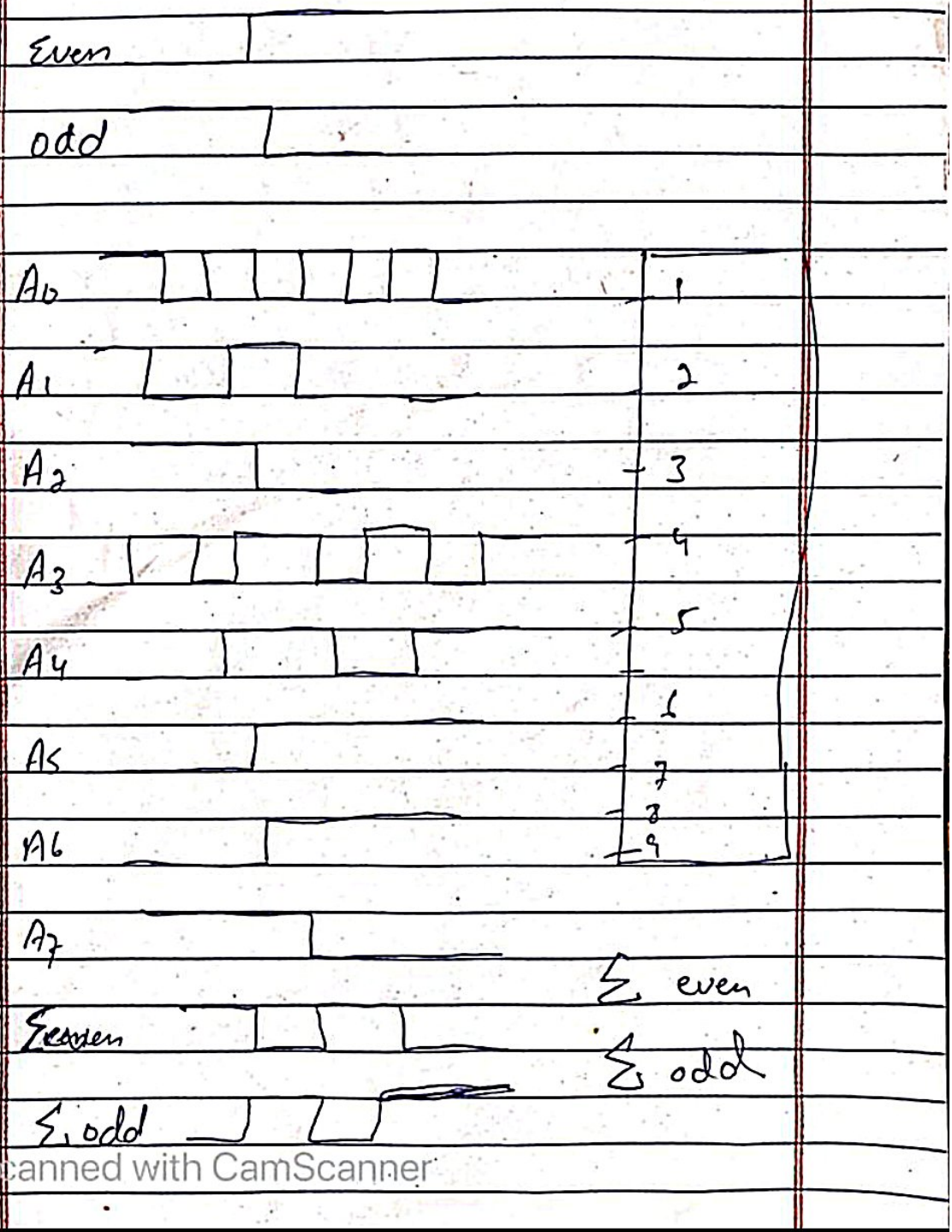
(Q3)



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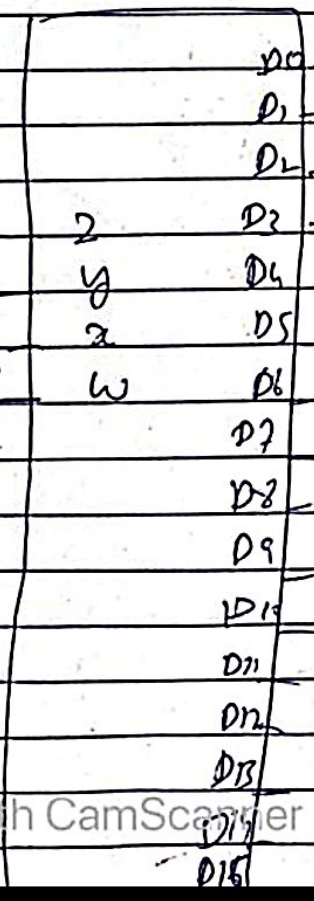
(Q7). (B) Explain 4-bit active low decoder.

4-bit active low decoder.

A decoder is a building block that takes in an n-bit binary number as input.

↳ Decodes that binary number as input the corresponding output.

↳ Individual output for every input combination i.e 2ⁿ output.



1 output for each combination of the input number.

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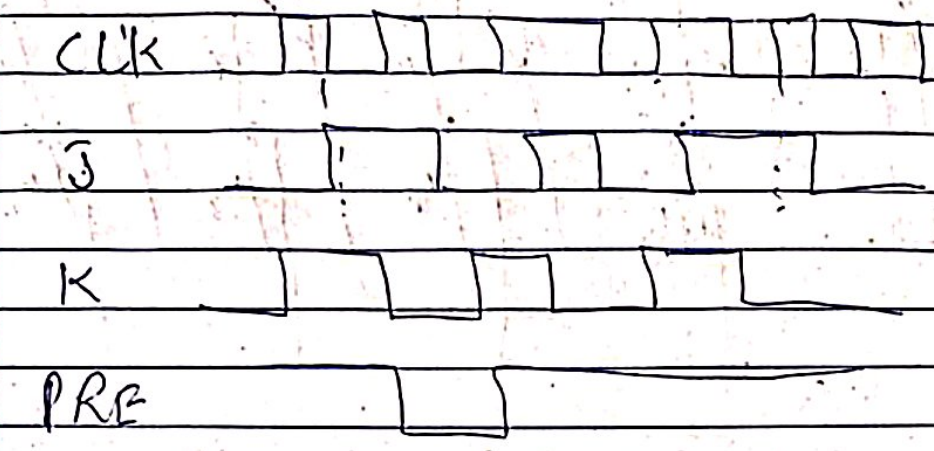
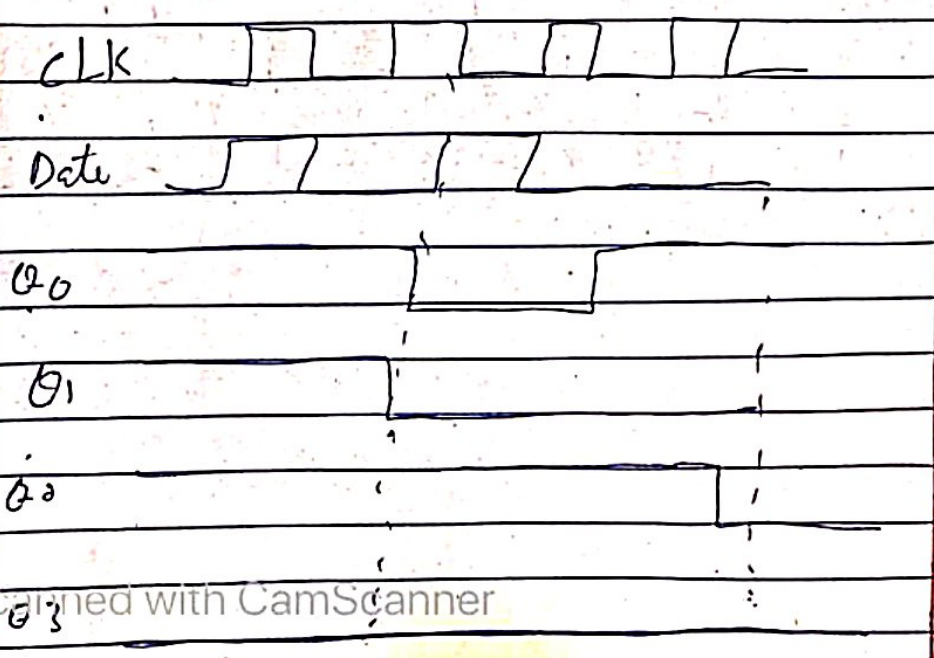
Q4



Q5



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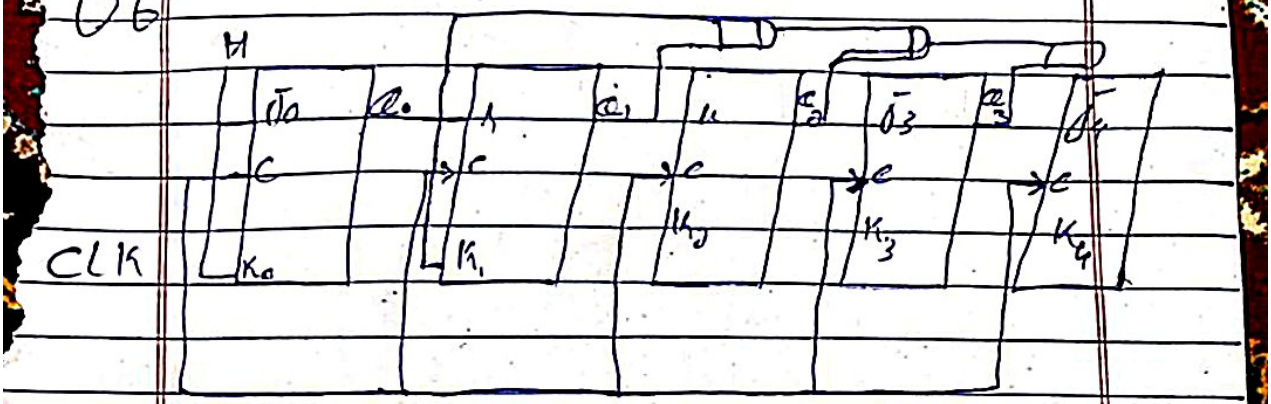

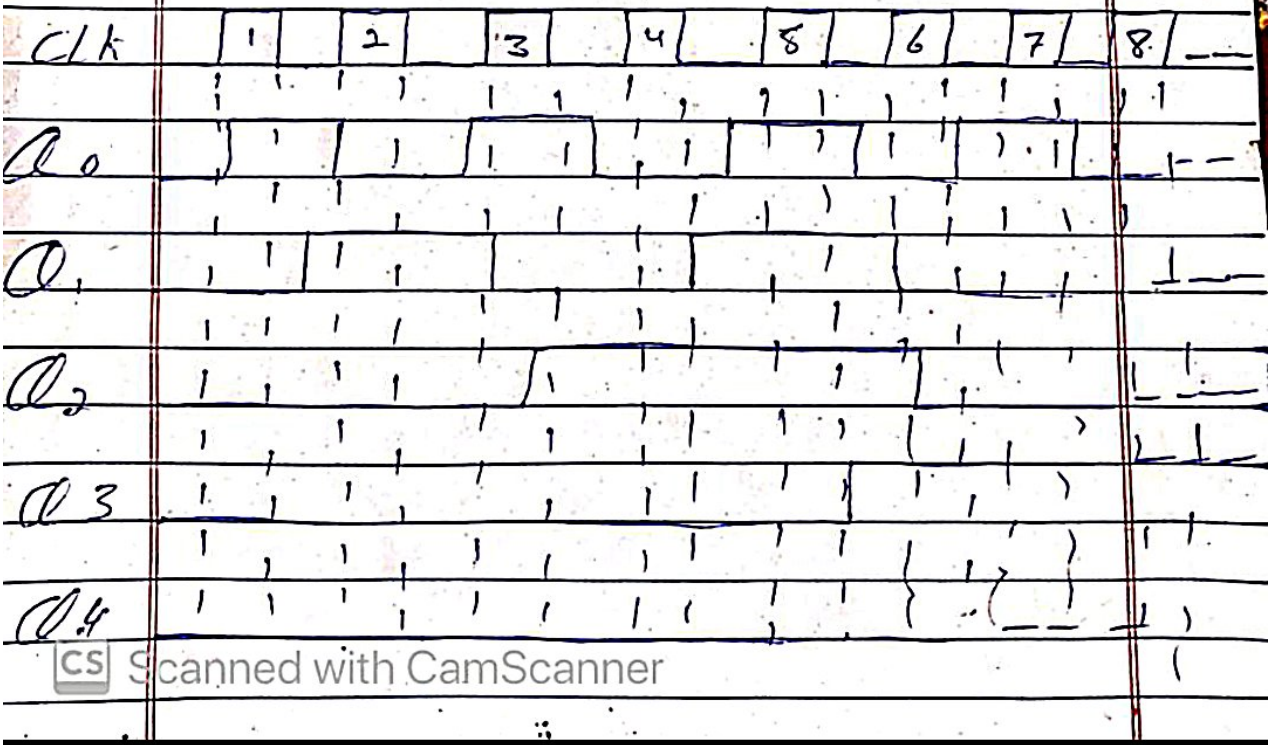

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