Programs: BC (CS), BS(SE), BS(TELC)

Subject: Digital Logic Design

Major Assignment Final-Term

Course Code: CSC-201

EDP Code: 102007016

Summer Semester 2020

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Q.1 Draw and explain the logic diagram for each of the following:

a) A circuit for adding or subtracting two 4-bit numbers

b) 4-bit active low decoder

c) Decimal to BCD encoder

d) Frequency divider (Use 3 J-K flip-flops and assume 16 kHz frequency of the initial wave-form.)

Q.2 For the 4-input multiplexer, data inputs are given as:

$D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find the output Y if the select inputs are given as:

Q.3 Timing diagram in Figure 01 shows inputs to a 9-bit parity checker. Draw the ∑ Even and ∑ Odd output for the even parity checking.

Q.4 The waveforms in Figure 02 are applied to the J, K, CLK, $\overline{PRE}$, and $\overline{CLR}$ inputs as indicated. Determine the Q output, if the flip-flop is initially RESET.

Q.5 Use the waveforms in Figure 03 to draw the timing diagram for the parallel outputs(Q_1, Q_2, Q_3, Q_4) for the shift register. Assume that register is initially cleared.

Q.6 Draw the logic diagram and timing diagram for the 4-stage synchronous binary counter. Verify that the waveforms of the Q outputs represent the proper binary number after each clock pulse.

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Submitted to Sir. Amin

Date 22-Sep. 2020

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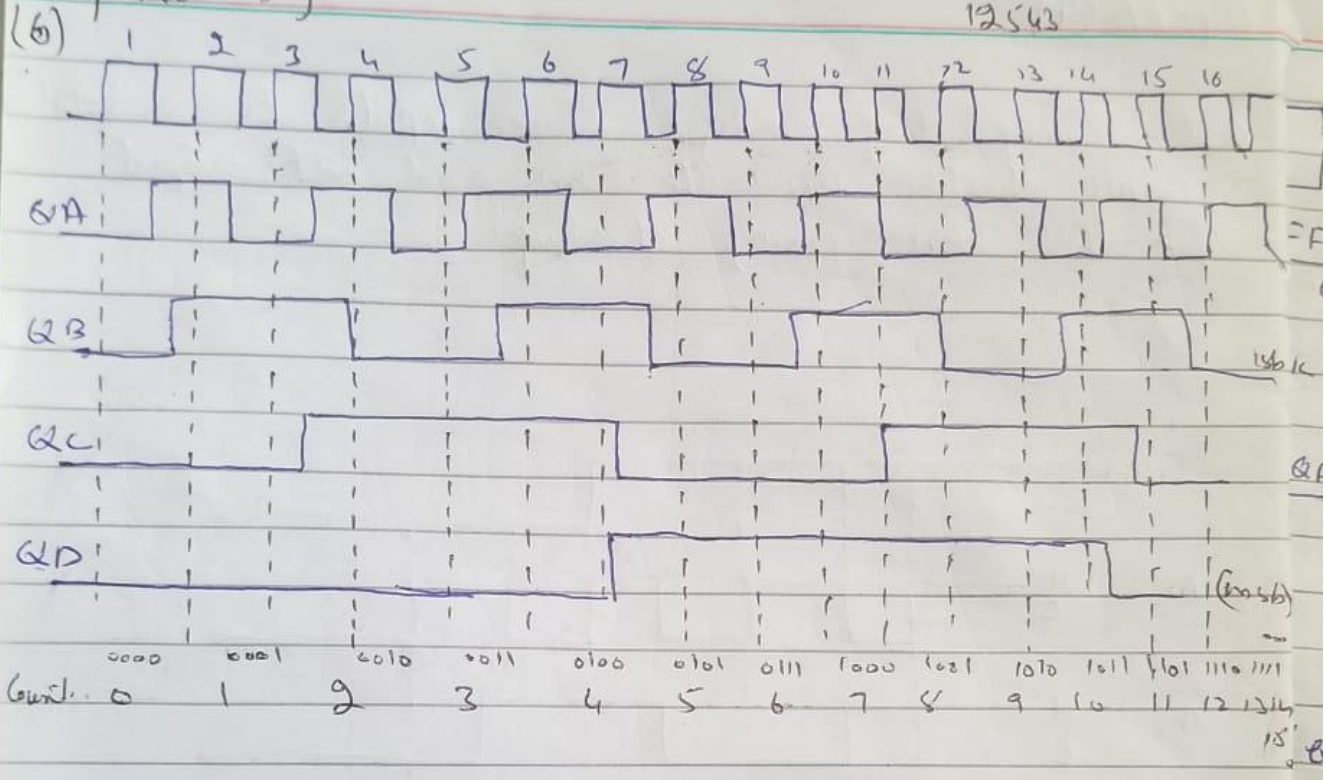

Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0(0000) to 15(1111). therfore this type of counter is also known as a 4-bit synchronous up counter.

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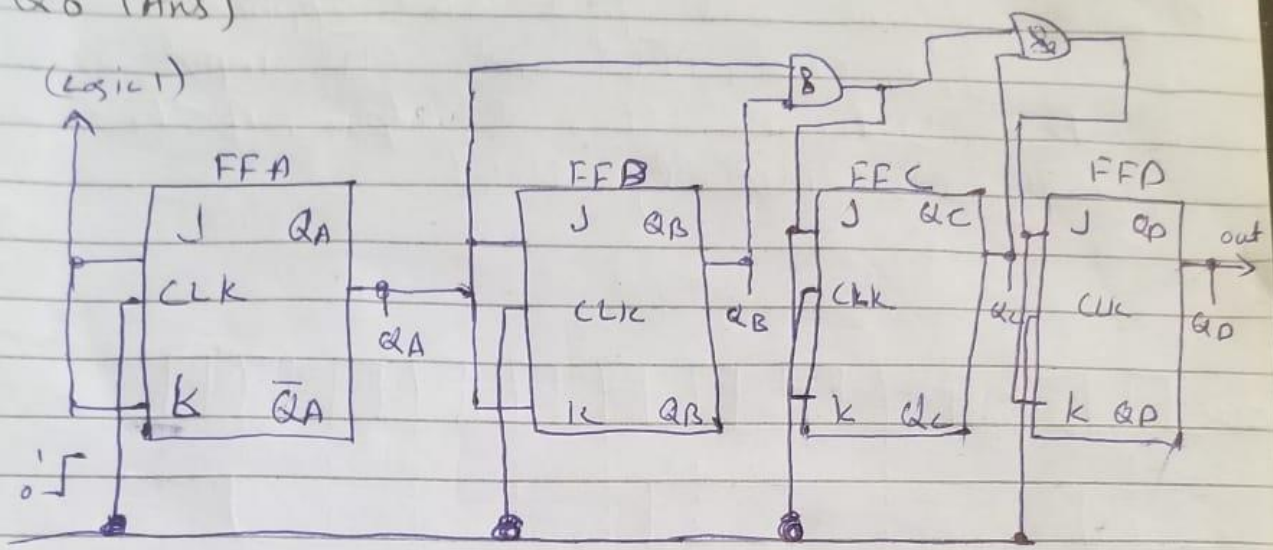
Q6 (Ans)



it can be seen above, that the external clock pulses are fed directly to each of the J-K flipflops in the counter chain and that both the J and K inputs.

the J and K inputs of flip-flop FFB are connected to the output Q_A of FFA but the J and K inputs of FFC and FFD are driven from seprat AND gates which also supplies with signals from the input and output of the previous stages

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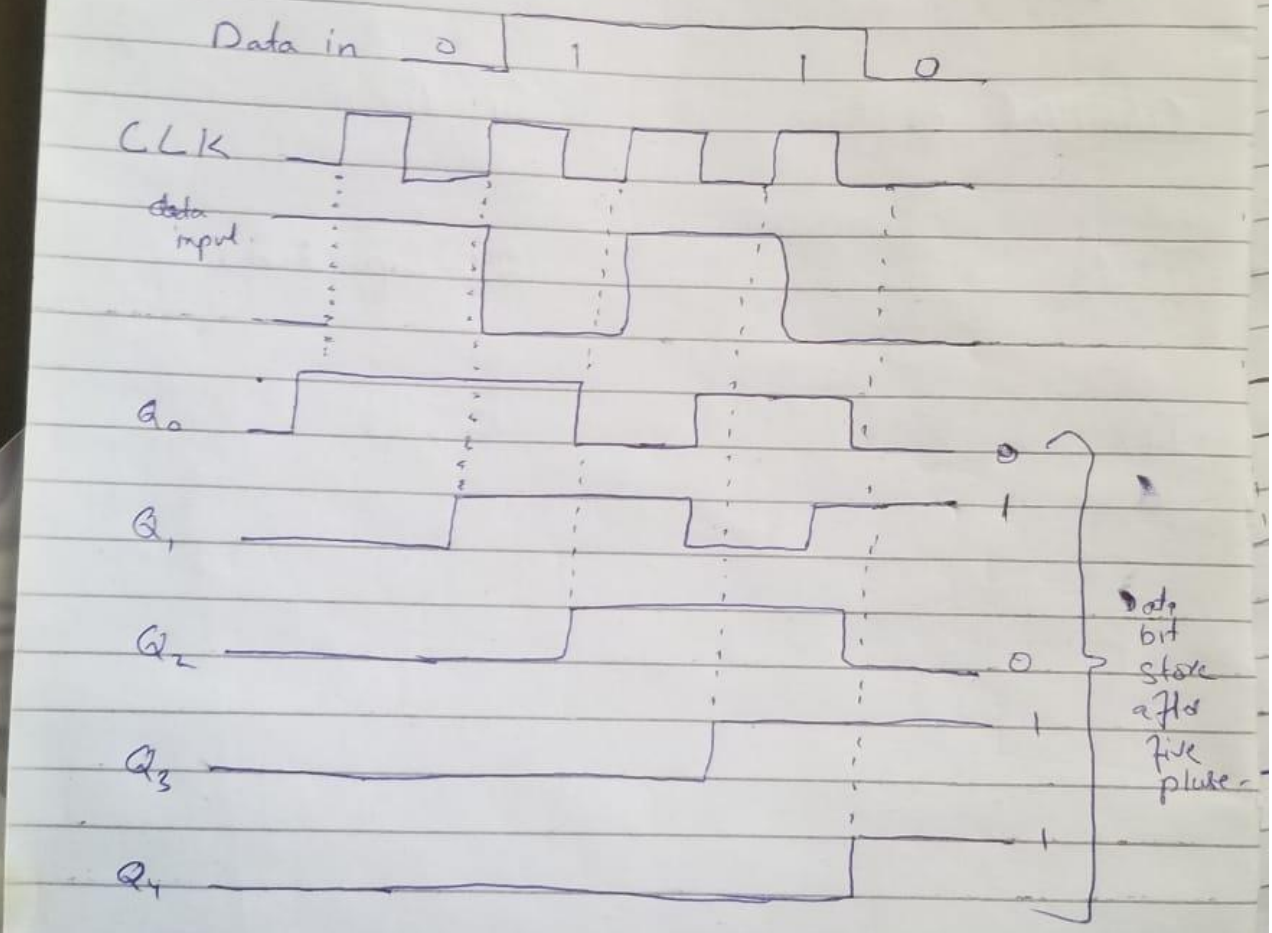
Q5 use the waveforms in Fig-3 to draw the timming diag for the parallel outputs (Q_1, Q_2, Q_3, Q_4) for the shift register - Assume that register is initially cleared.



the first data bit entred into the register on the first clock Pulse and then shifted from left to right as the remaining bits entred and shifted. the register contains Q_4, Q_3, Q_2, Q_1, Q_0 = 11010 after five clockpulses

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Q4 The waveforms in Fig 2 are applied to the J, K, CLK, $\overline{PRE}$ and $\overline{CLR}$ input as indicated. Determine the Q output, if the flip-flop is initially Reset.

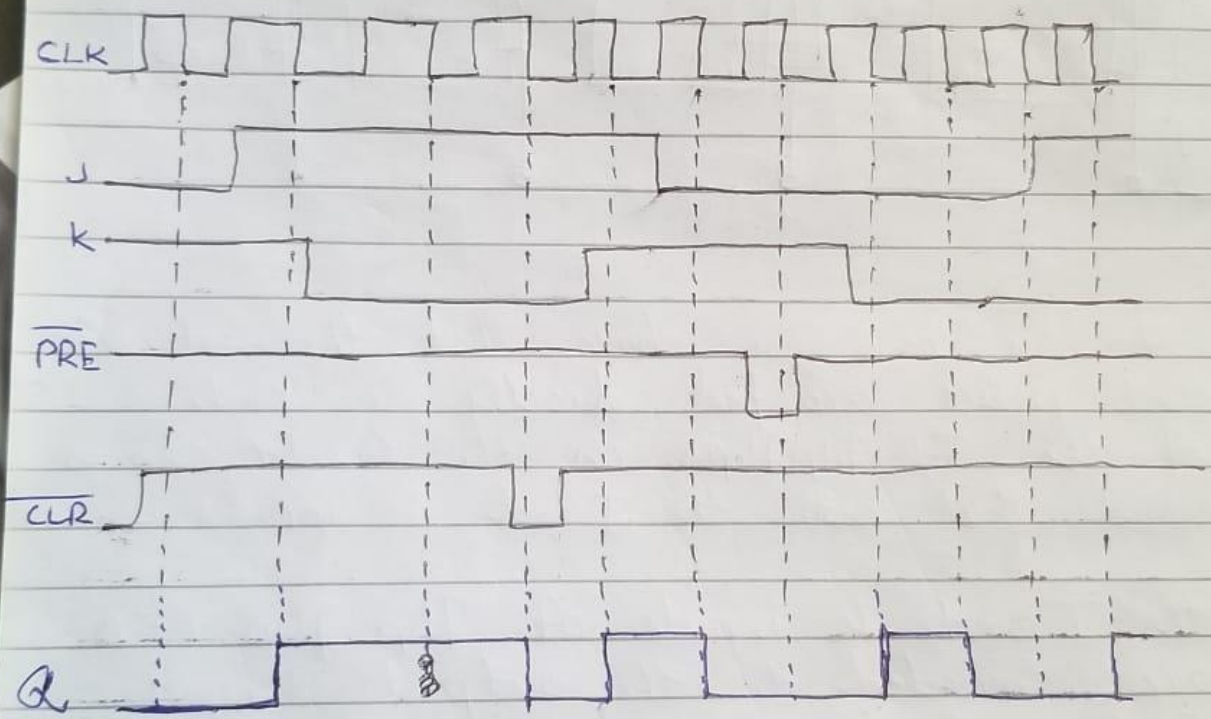
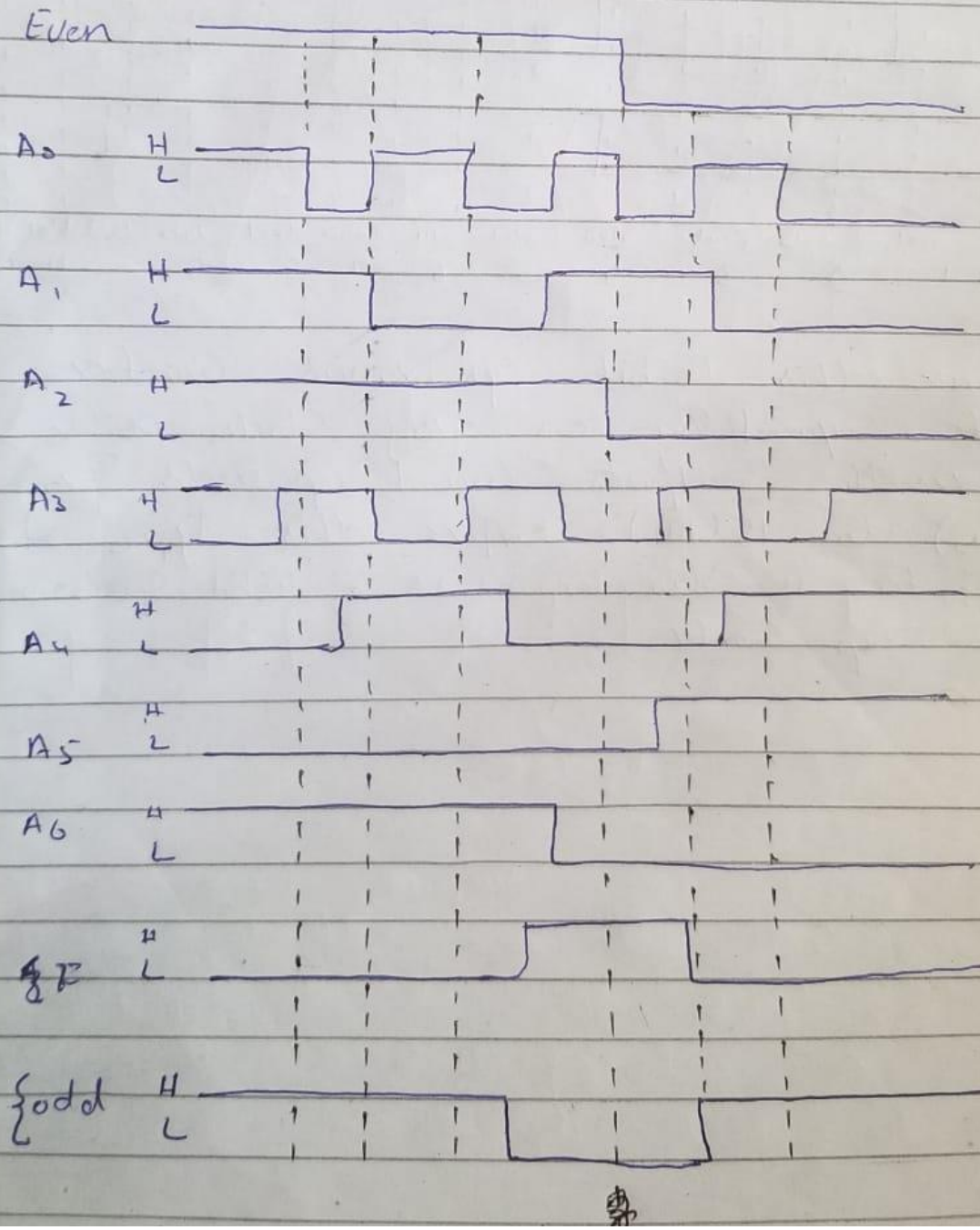


Fig (2)

The resulting Q waveform shown in Fig(2) Notice that each time a Low is applied to the $\overline{PRE}$ or $\overline{CLR}$, the flip-flop is set or reset regardless of the states of the other inputs.

Q3(Timing diag in fig 1 shows inputs to a 9-bi parity checker. Draw the Even and odd output for the even parity checking.



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Q2: For the 4-input multiplexer, data inputs are $D_0 = 0$, $D_1 = 1$, $D_2 = 0$, $D_3 = 1$

Find output y if.

$S_0 = 1$ $S_1 = 0$

$S_0 = 0$ $S_1 = 1$

$S_0 = 1$ $S_1 = 1$

$S_0 = 0$ $S_1 = 0$

Sol

A 4x1 Mux has 4 input lines (D_0, D_1, D_2, D_3) two select input (S_0 and S_1) and one out put line Y.

if $S_1 S_0 = 00$ then $Y = D_0$

if $S_1 S_0 = 01$ then $Y = D_1$

if $S_1 S_0 = 10$ then $Y = D_2$

if $S_1 S_0 = 11$ then $Y = D_3$

Data input		output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Truth table.

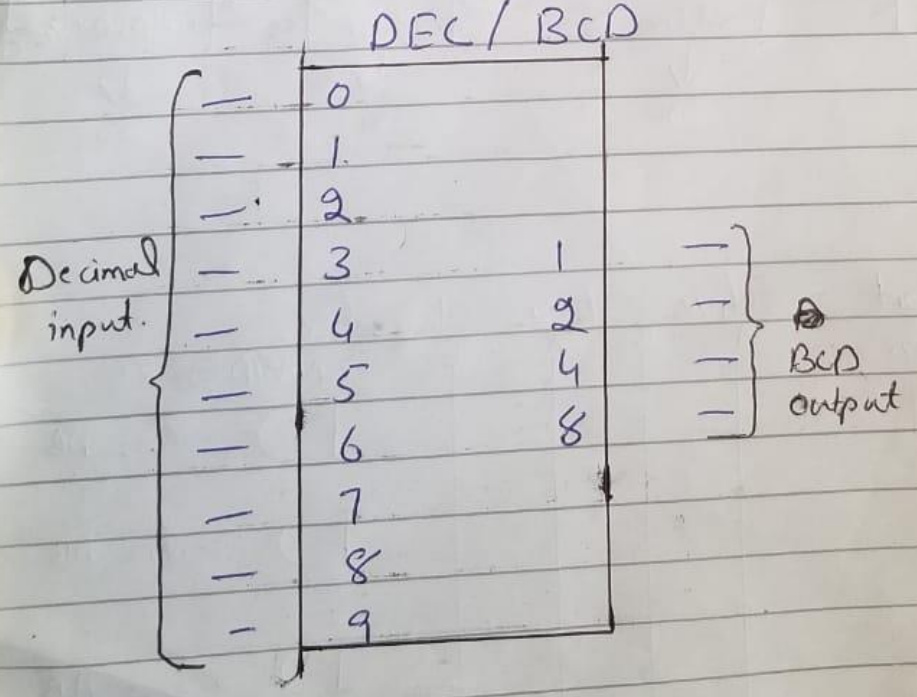
A	B	Q_0	Q_1	Q_2	Q_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Q1 (part c)

Decimal to BCD encoder.

Sol:

- encoder has ten inputs - one for each decimal digit and four outputs the outputs indicate the BCD code that represend the active input.



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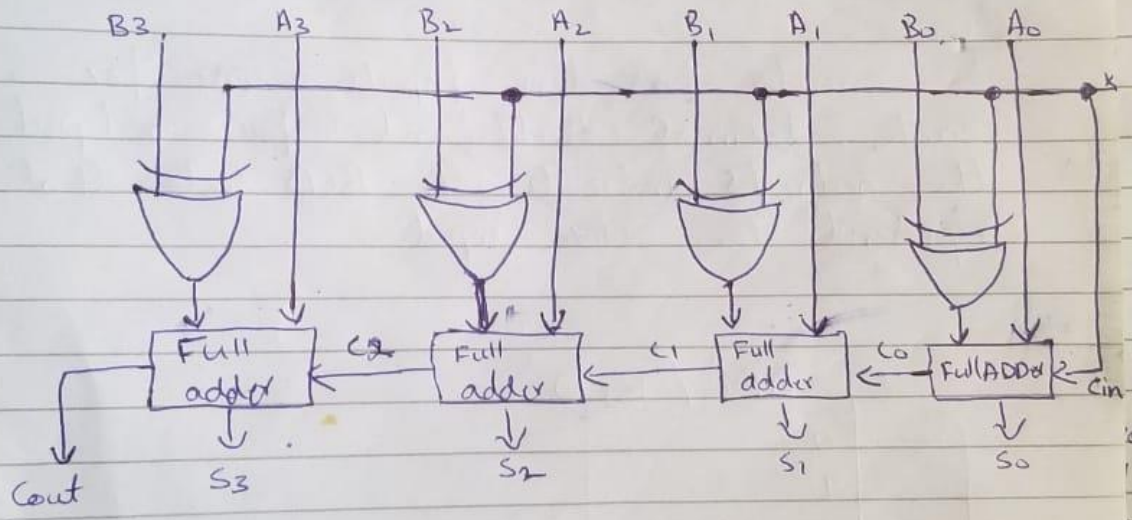
(Q1) Draw and explain the logic diagram

(a) A Circuit for adding or Subtracting two 4-bit numbers.

Ans In Digital Circuit, A binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers is one Circuit itself. it is one of the components of (ALU)



Q(1)(b)

4 bit active low decoder.