:: ASSIGNMENT # 5 ::

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Subject: Computer Architecture

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Q1 Give detail answer to each of the following.

(a) Discuss different types of semiconductor memories in detail.

Types of semiconductor memories.

There are various types of semiconductor memories. The most common is ~~Expanded~~ referred to as RAM (Random access Memory). Most types have the property of Random Access Memory which means that it take the same amount of time to access any memory location. Below ill make a table to explain different types of.

Memory type	Category	Erasure	Write mechanism	Volatility
RAM (random memory)	Read/write memory	Electrically Byte level	Electrically	volatile
ROM	Read only memory	Not possible	Masks	Non Volatile
PROM	"	"	"	"
EPROM	"	UV light chip level	"	"
EEPROM	"	Electrically byte level	"	"
Flash Memory	Read Mostly Memory	Electrically block level	Electrically	"

(b) Explain the read and write operation for the SRAM...

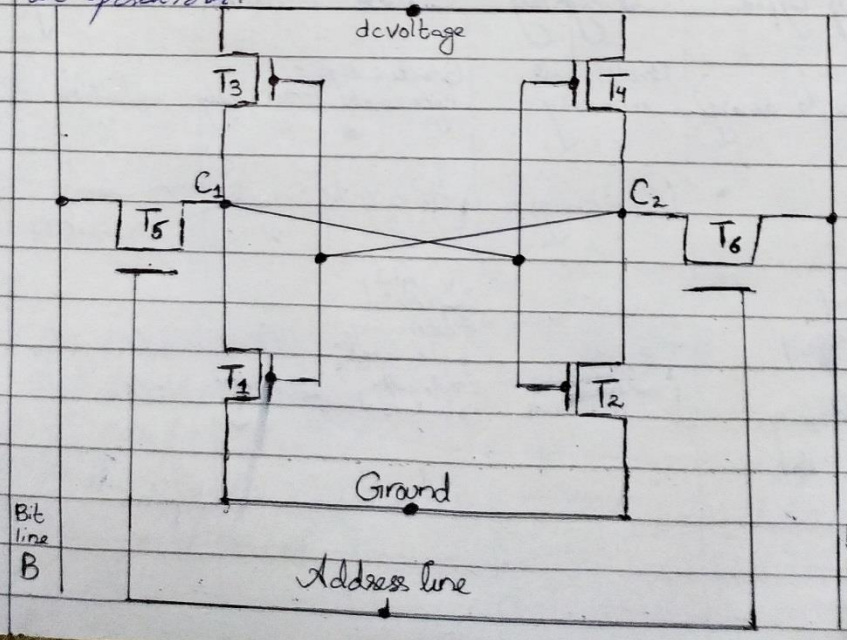
Answer:

Read Operation:

In SRAM, for any operation to be performed the word line should be high. To perform read operation, initially a voltage signal is applied to the bit line. High voltage represents 1, and a low voltage represents 0.

Write Operation:

Consider the memory bits consists of Q=0 and $\overline{Q}$=1. When the address line is selected, the transistors turn on and the charge stored on the capacitor is fed out onto a bit line and to a sense amplifier if the cell contains a logic 1 or a logic 0. The readout from the cell discharges the capacitor which must be restored to complete the operation.



c) Explain the read and write. - - -.

Read Operation:

When the address line is selected, the transistor turns on and the charge stored on the capacitor is fed out onto a bit line & to a sense amplifier. It compares the capacitor voltage to a reference value & determines if the cell contains a logic 1 or a logic 0.

Write operation:

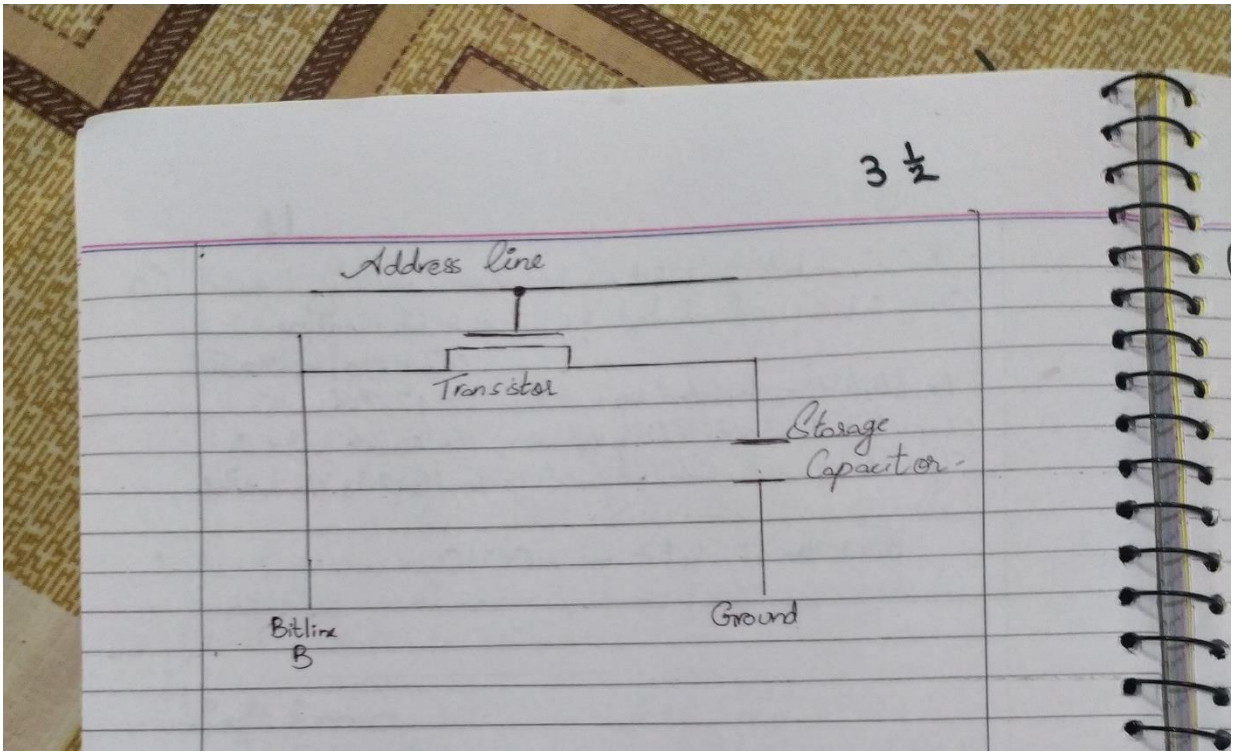
A voltage signal is applied to a bit line a high voltage represents 1 & a low represents 0.

d) Discuss 16 Mbit. . - ---.

In the Case of this diagram.

- 4 bits are read as written at a time
- Memory array is organized as four arrays of 2048 by 2048 elements.
- Address lines supply the address of the word to be selected log 2. W lines are needed
- These lines are fed into a row decoder
- Decoder activates a single line of memory
- The same procedure is applied to select columns.
- Note that there are ~~not~~ only 11 address lines (A0 - A10)
  - Half the number you would expect for a 2048 x 2048 array
- First, a row address select (RAS) signal is emitted

THIS IS THE DIAGRAM OF PART C I FORGOT TO MAKE IT IN START SO MADE IT IN THE END AND INSERTED IT HERE…….



- to define the row address of the array.

Second a column address select (CAS) signal is emitted:
- to define the column address of the array.

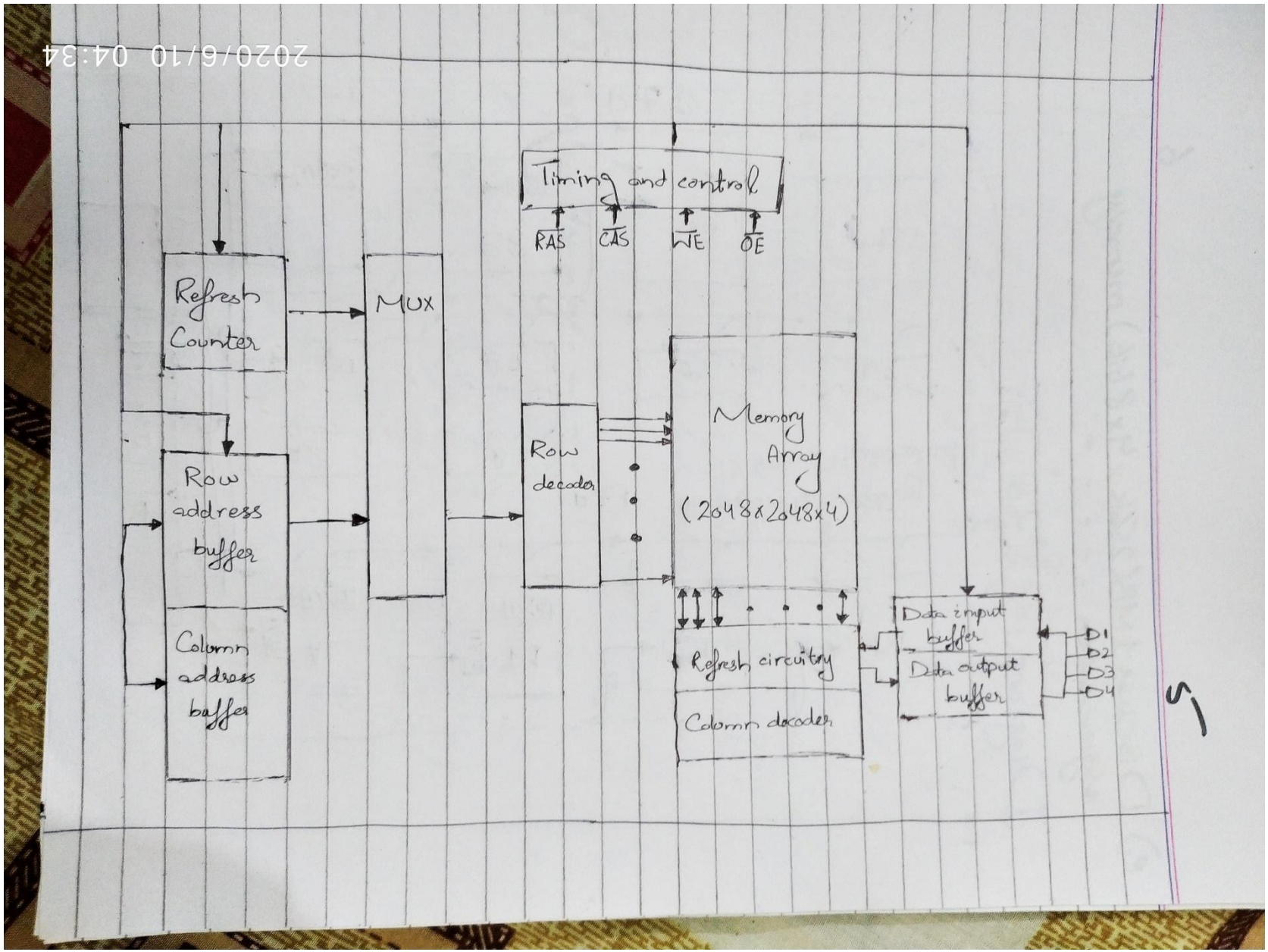
Write enable (WE) signal
- Specifies that a write operation is to be performed.

Output enable (OE) signal
- Signal that specifies that a read operation is to be performed.

Refreshing technique:
- Refresh counter: step through all of the row values.

For each line:
- Memory row is chosen, RAS line is activated and Data are read out and written back into the same location.

Discuss


Timing and control
RAS
CAS
WE
OE
Refresh Counter
MUX
Row address buffer
Column address buffer
Row decoder
Memory Array
(2048x2048x4)
Refresh circuitry
Column decoder
Data input buffer
Data output buffer
D1
D2
D3
D4

e) Discuss 1MB (256k x 4x8 bit) memory organization . . . . .

Diagram

Explaination:

$(1M \times 8bit / 256K \times 8bit) = 4 = 2^2$

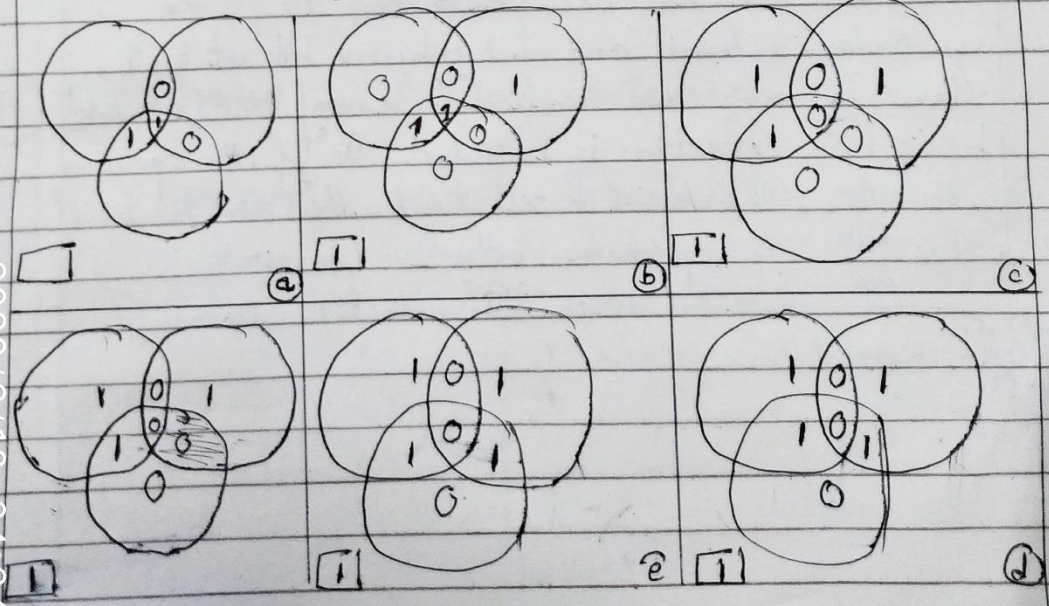
As shown in the figure 1M word by 8bits per word is organized as four columns of chips each column containing 256K words arranged as in prev figure

- $1M = 2^{20}$

For 1M word, 20 address lines are needed The 18 least significant bits are routed to all 32 modules.

The highest order 2 bits are input to a group select logic module that sends a chip enable signal to one of the four columns of modules.

8) Explain Hamming - - - -



With 1 bit per chip organization an SEC DEC code is generally considered adequate e.g the IBM 30xx implementations used an 8 bit SEC-DEC code for each 64 bits of data in main memory. The size of main memory is actually about 12% larger than is apparent to the user. The VAX computers used a 7 bit SEC-DED for each 32 bits of memory, for a 22% overhead.

g) How is the syndrome for hamming - - -

Answer:

A syndrome is created by the XOR of the code in a word with a calculated version of that code. Each bit of the syndrome is 0 or 1 according to if there is or is not a match in that bit position for the two inputs. If the syndrome contains all 0s, no error has been detected. If the syndrome contains one and only one bit set to 1, then an error has occured in one of the 4 check bits. No correction is needed. If the syndrome contains more than one bit set to 1, then the numerical value of the syndrome indicates the position of the data bit in error. This data bit is inverted for correction.

Q² Differentiate each of the following:

a) DRAM and SRAM:

DRAM	SRAM
• DRAM is more dense and less expensive	• SRAM is expensive.
• DRAM requires the supporting refreshing circuitry	SRAM does not require any refresh circuitry.
• DRAM are Normal in speed	SRAM are faster in speed than DRAM
• DRAM is used for main memory	SRAM is used for cache memory.

b) EEPROM and Flash Memory

EEPROM	Flash Memory
EEPROM devices can erase any byte of memory at any time	Flash memory can only erase an entire chunk or "Sector" of memory at a time.
EEPROM uses NOR type of memory	Flash memory uses NAND type memory.
EEPROM is bytewise erasable	Flash is block wise erasable.

c) Hard failure and . . - . - - - - . .

Hard Failure:

A hard failure is a permanent physical defect so that the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically b/w 0 and 1. Hard errors can be caused by harsh ~~envio~~ ~~error~~ environmental abuse, manufactoring defects and wear.

Soft Error:

Soft error is a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory. Soft errors can be caused by power supply problems or alpha particles.

Q3 Suppose an 8-bit data . . - - - . . - . . . - - -

Solution.

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	C8	D4	D3	D2	C4	D1	C2	C1
Black	1	0	1	0	-	1	0	1	-	0	-	-
Codes	1100	1011	1010	1001	1000	0111 ~~0110~~	0110 ~~0101~~	0101	0100	0011	0010	0001

The check bits are in bit numbers 8, 4, 2 and 1
Check bit 8 calculated by values in bit numbers
:12, 11, 10, and 9 = 0
Check bit 4 calculated by values in bit 12, 7, 6 and 5 = 1
Check bit 2 calculated by values in 11, 10, 7, 6 and 3 = 0
Check bit 1 calculated by values in 11, 9, 7, 5 and 3 = 0

Thus the check bit are : 0010