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Assignment no 5
Submitted to Sir Amin
Subject Computer Architecture
program BSCS
Department Computer Sci

Q= Give detail ans to each of the following.

(a) Discuss different types of Semi-conductor memories in detail.

There are various types of Semi-conductor memories. The most common is keffered to as RAM. Most type have the property of random Access memories which mean that it takes the same amount of time to access any memory location.

* Here is the table of Semi-conductor memory types.

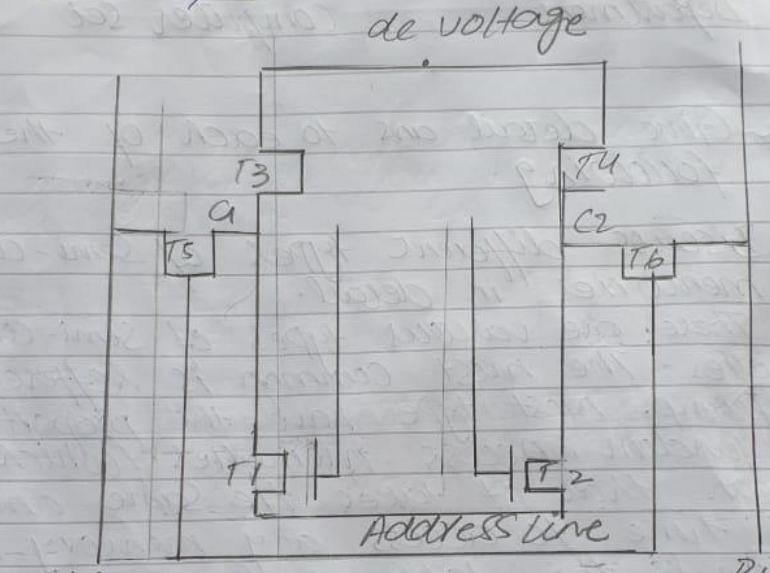
Memory types	Category	Erasure	Write mechanism	Volatility
RAM (random memory)	Read/write memory	Electrically byte level	Electrically	Volatile
ROM	Read only memory	Not possible	Masks	
PROM		using typo chip level		
EPROM		electrically level		
EEPROM	Read most memory	electrically block level	Elec-trically	Non volatile
Flash memory				

(b) Explain the read & write operation for the SRAM cell using diagram read operation.

In SRAM for only operation to be performed performed the word line should be high. To perform read operation initially

* write operation

Consider the memory bits consists of Q=0 & Q=1



Static ram (SRAM) cell

(C) Explain the read & write operation the DRAM cell using cell diagram

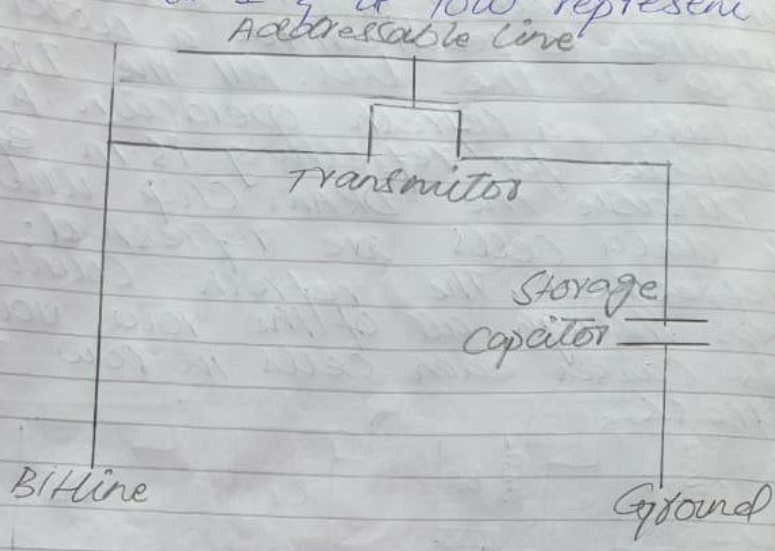
read operation

When the address line is selected the transistors turn on & the charged stored on the capacitor is fed out onto a bit line & to a sense amplifier if compare the capacitor voltage to a reference value & determine if the cell contains a logic 1 or a logic 0.

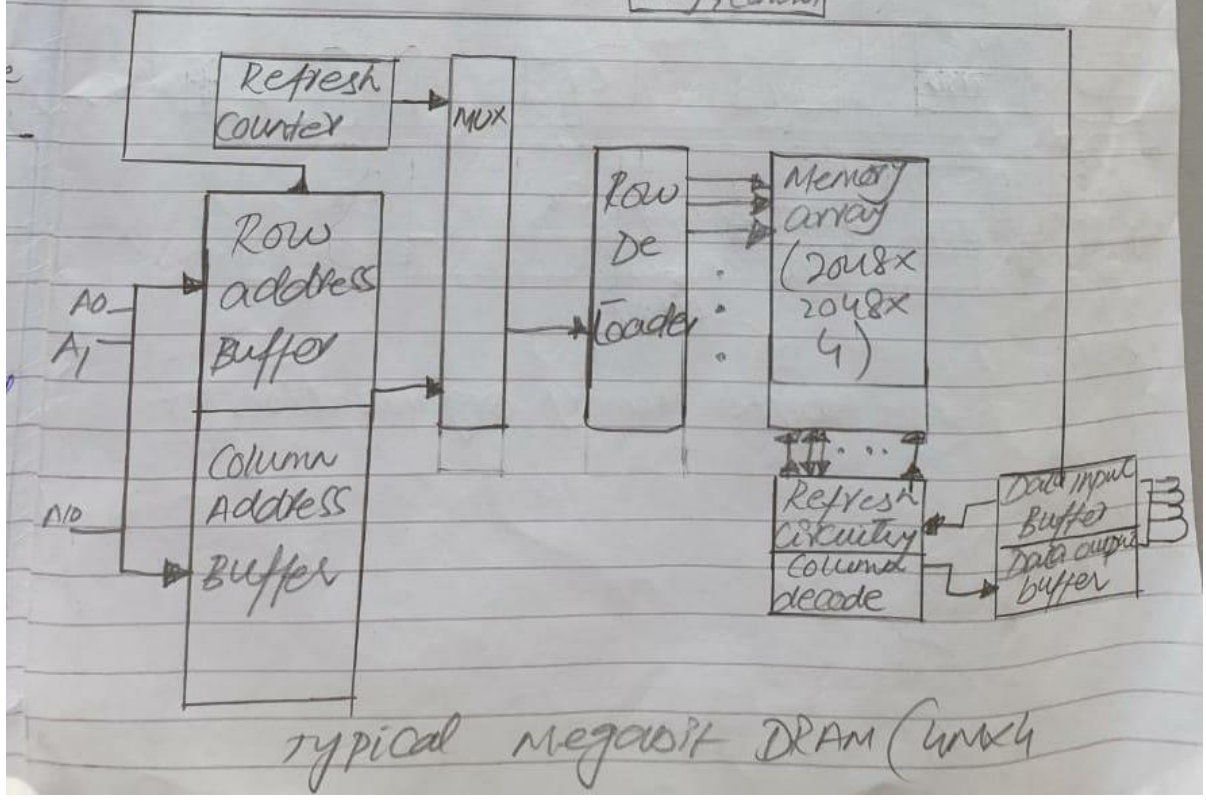
* write operation.

(3)

A voltage signal is applied to a bit line a high voltage represents 1 & a low represent 0

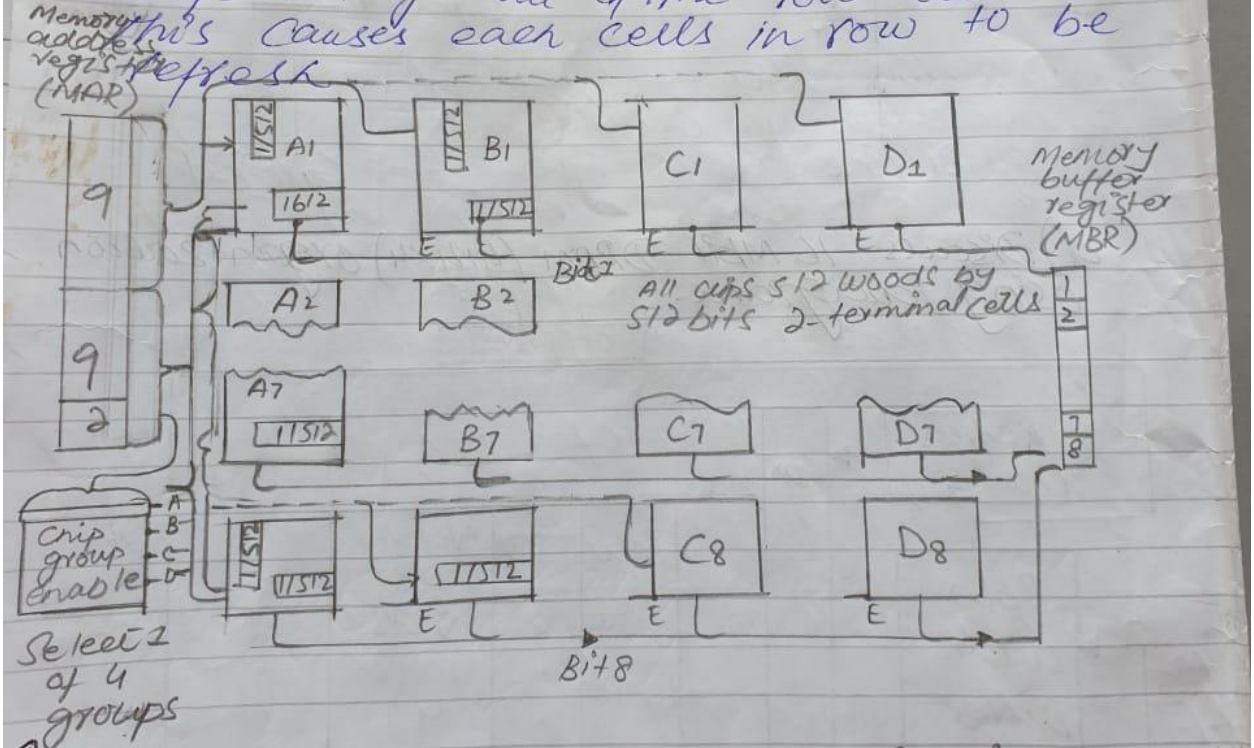


d) Discuss 16-Mbit DRAM (4194x4) organization using diagram.



Typical Megabit DRAM (4Mx4

Because only 4 bits are read/written to their DRAM there must be multiple DRAMs connected to the memory Controller to read/written a word of data to the bus. All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM chip while all data cells are refreshed. The refreshed. The refresh counter steps through all of the row values. This causes each cells in row to be refresh

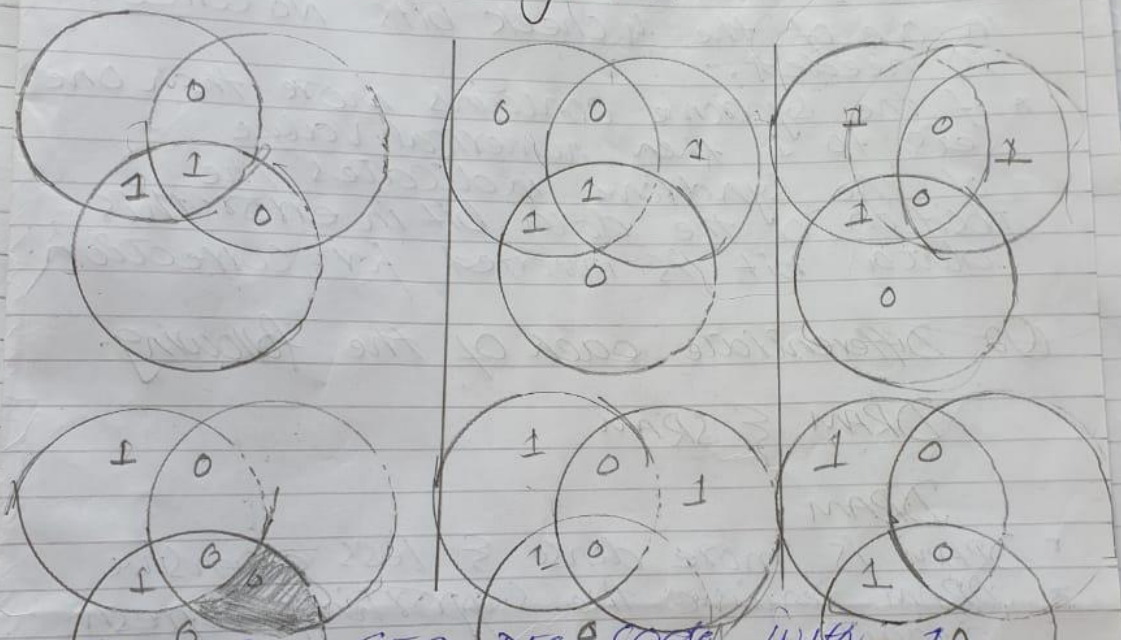


1 - Mbyte Memory organization

c) Discuss 1MB (256K x 4 x 8Bit) memory organization using diagram

The possible organization is received of a memory consisting of 1M word by 8 bits per word. In this case we have four colums of chips, each column containing 256K words arranged.

(f) Explain Hamming SEC-DEC code using venn diagrams



Hamming SEC-DEC code with 10 bit per chip organization an SEC-DEC code is generally considred adequate e.g the IBM 30xx implementation used an 8 bits SEC-DEC code for each 64bits of data in main memory. The size of main memory is actuddly about 12% larger than is apperent to the user The vax computer used a bits SEC-DEC for each 32 bits of memory for a each 32 bits of memory for a 22% overhead.

9) How is Syndrome for the having code interpreted.
Syndrome for the haming code interpreted as follows.
* If the Sydrome contains all 0s no error has been detected.
* if Sydrome contains one & only one bit set to 1 then an error has occured in one of the 4 check bits No correction is needed.
* if the Sydrome contains more than one sets to 1 then numerical value of the Syndrome indicates the position of the data bit in error. this data bit is inverted for correction.

Q2 Differentiate each of the following.

DRAM & SRAM

DRAM
* DRAM is more dense & less expensive
* DRAM requires the supporting refresh ciscuitry.
* DRAM are normal in Speed.
* SRAM is used for cache memory.

SRAM
* SRAM is expensive
* SRAM doesn't require any refresh ciscuitry
* SRAM are faster in speed than DRAM
* DRAM is used for main memory

b) EEPROM & flash memory

* EEPR
eras
memo
* EEPR
mem
* EEPR
era

(7)

* EEPROM devices can erase any byte of memory at any time * EEPROM uses NOR type memory * EEPROM is byte-wise erasable	* Flash memory can only erase an entire chunk or sector of memory at a time. * Flash memory uses Nand type memory * Flash is block-wise erasable.

Q NO# 3

$m = 8$

$2^k - 1 >= k + m$

$2^4 - 1 >= 4 + 8$

$15 >= 12$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

* The check bits are in bit numbers 1, 2, 4 & 8
* Check bit 8 calculated by values in bit numbers: 9, 10, 11, & 12
* Check bit 4 calculated by values in bit numbers: 5, 6, 7, & 12.
* Check bit 2 calculated by values in bit numbers: 3, 6, 7, 10 & 11
* Check bit 1 calculated by values in bit numbers: 3, 5, 7, 9, 10, 11

Thus the check bits are: 1011