Department of Electrical Engineering
Assignment
Date:

14/04/2020

Course Details

Course Title: Electronic Circuit Design
Module: 04
Instructor: Eng Mujtaba Ihsan
Total Marks: 30

Student Details

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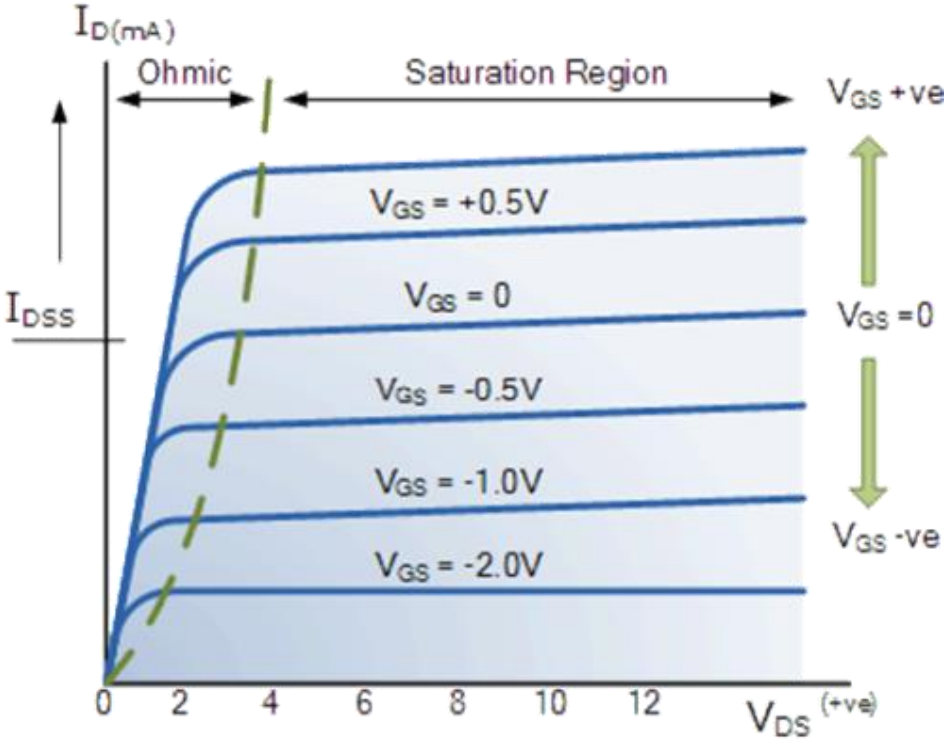
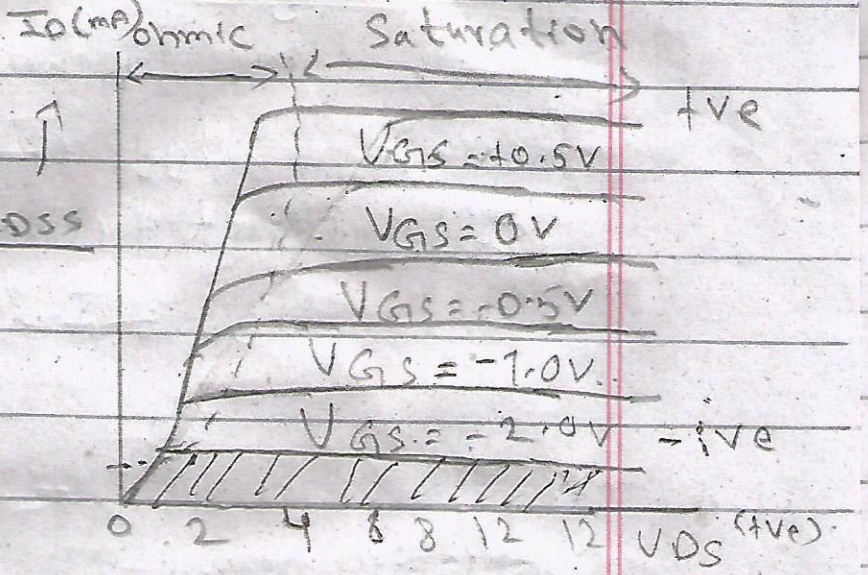
Student ID: 15006

Q 1.	(a)	**Explain** the drain characteristic curve of D-MOSFET given below.  	Marks 07 CLO 1

Q1:-

Ans:- (1)



In the above drain characteristic curve.

IDss :- It is the maximum drain current that an FET produces.

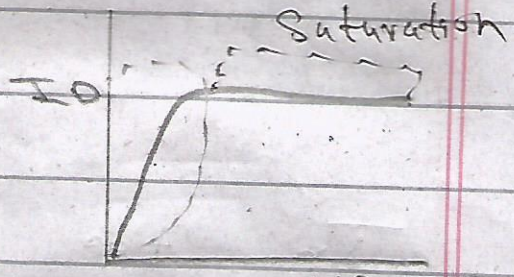
(i) If we keep VGs (Gate to Source Voltage) at 0 Volt if we increase VDs, ID also increase (Here we consider electronic current)

$\bar{e}$ flows from S to Drain

Ohmic Region:- It follows ohm's law because if we increase V_{DS} . I_D also increases so. direct relation.

$$V_{DS} \propto I_D$$

Saturation region:-

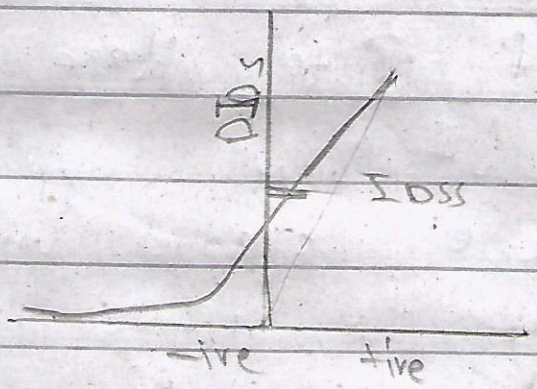


In this region the transistor will be biased so max ~~curr~~ amount of gate voltage is applied to the device. so max current flowing through the mosfet switch.

Cut off region:- In this region the transistor. It is the condition of zero input voltage.

So from the graph the transistor is N-channel D Mosfet it means that it required $-V_{GS}$ to switch the transistor off

The D-mosfet operate as Depletion mode when $-V_{GS}$ is applied or act as Enhancement mode when tive V_{GS} is applied

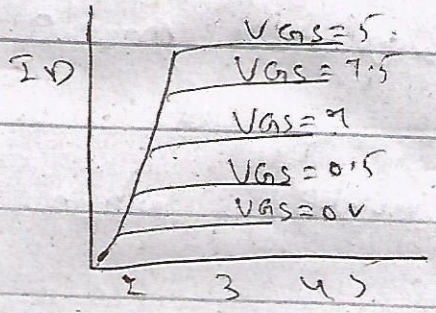


So from the graph

(i) when V_{GS} is at 0V when we increase V_{DS} ther is almost const current I_D also increase here we consider electronic current

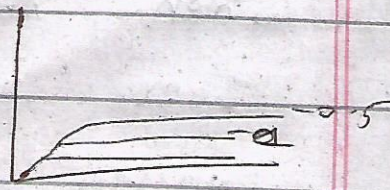
if Gate voltage +ive:- If the gate voltage is +ive the channel width increases as a result ID through channels increases.

As we look to the graph when we apply Vgs 0.5V the ID also increases



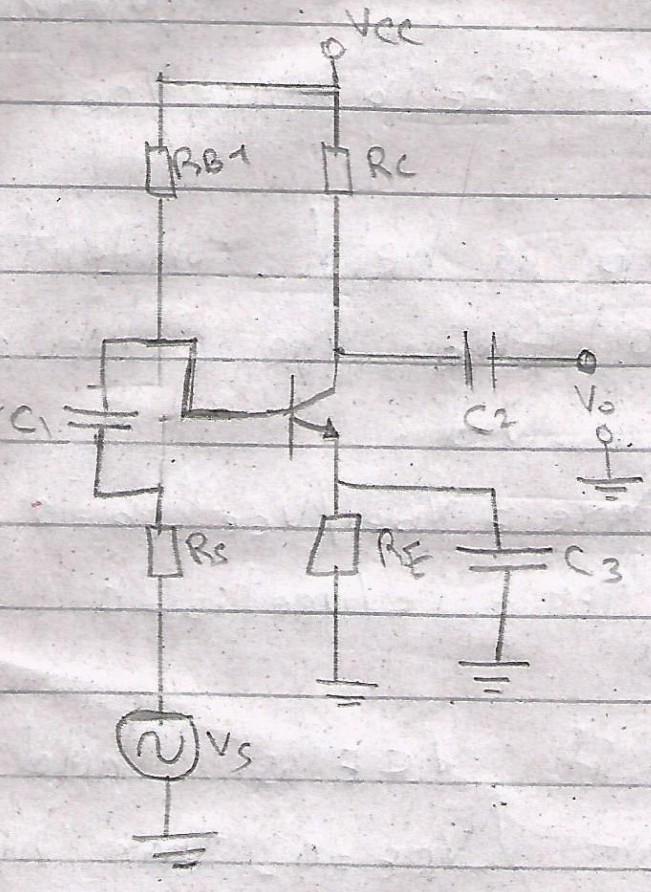
If Gate voltage is -ive:-

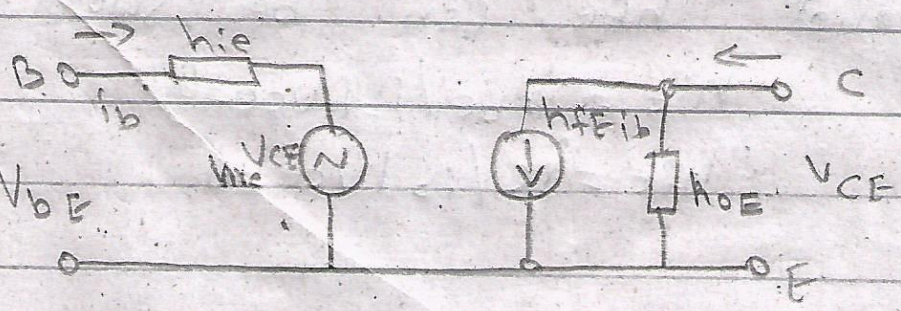
If we apply -ive voltage the channel width decreases as a result very little decreases. If keep them more -ive so the transistor are in the cut off region. or turned off.



(b)	**Sketch** the hybrid model and write equations for the transistor in common emitter configuration.	Marks 06	CLO 1

Ans b:- Transistor Hybrid Model:-





hie input impedance (Ω)
hre reverse voltage ratio (dimensionless)
hfe forward current transfer ratio (--)
hoe output admittance (siemen

input voltage equation:- V_{be}

$$V_{be} = h_{ie} i_b + h_{re} V_{ce}$$

Output voltage equation :- i_c

$$i_c = h_{fe} i_b + h_{oe} V_{ce}$$

if i_b is held constant ($i_b = 0$) then h_{re} & h_{oe} can be solved

$$h_{re} = V_{be} / V_{ce} \,|\, i_b = 0$$

$$h_{oe} = i_c / V_{ce} \,|\, i_b = 0$$

Also if V_{CE} is held constant ($V_{CE} = 0$) than h_{ie} and h_{fe} can be solved :-

$$h_{ie} = V_{be} / i_b \,|\, V_{ce} = 0$$

$$h_{fe} = i_c / i_b \,|\, V_{ce} = 0$$

Q 2.		A certain operational amplifier has a common mode gain of 0.6 and an open loop differential voltage gain of 400,000. **Evaluate** the CMRR & express it in decibels.	Marks 05
			CLO 2

Q 2:-

Given data :-

Common mode gain = 0.6

differential voltage gain = 4000,000

find :- CMRR = ?

expresse in decibels = ?

$$CMRR = Ad/Ac$$

Ad = differential voltage gain

Ac = common mode gain

$$CMRR = Ad/Ac$$

$$= \frac{4000,000}{0.6}$$

$$= 6666666.667$$

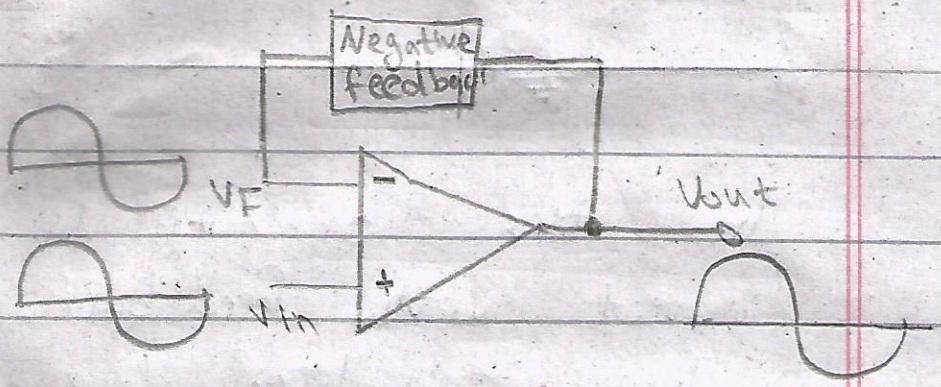
$$CMRR(dB) = 20 \times \log_{10}(CMRR)$$

$$= 156.47817 \text{ dB}$$

Q 3.	(a)	**Explain** the concept behind negative feedback in operational amplifiers.	Marks 06
			CLO 2

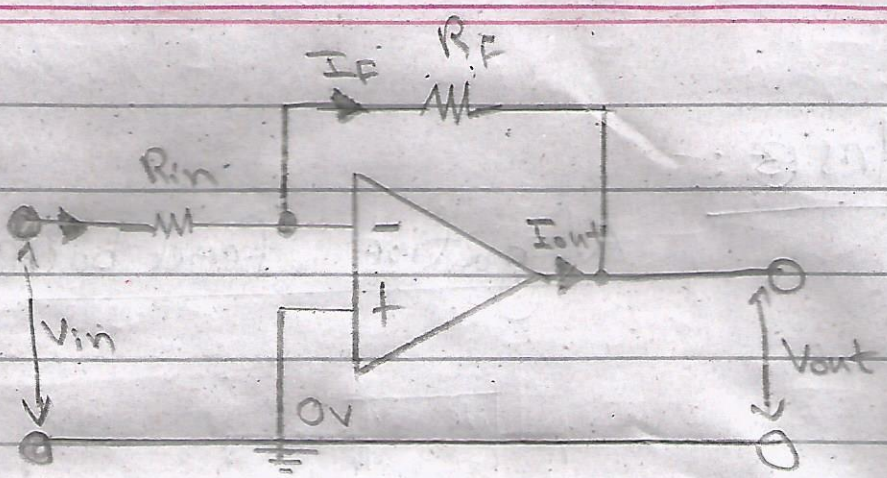
Ans ③ :-

Negative feed back:-



" Negative feed-back is the Process of "feeding back" a fraction of the output signal back into input, but to make the feed back -ive we must feed it back to the -ive or (inverting input) terminal of the op-amp using an external Feed back Resistor R_F

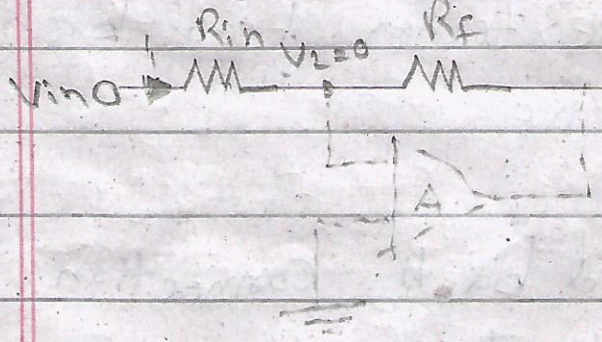
This feed back connection b/w the output & the inverting input terminal forces differential to zero.



In this OP-Amp is connect with feed back to produce a closed loop operation

Two rules to remember about Inverting amplifier

- No Current flows into the input terminal
- The differential Input voltage is zero as $V_1 = V_2 = 0$ (virtual earth)

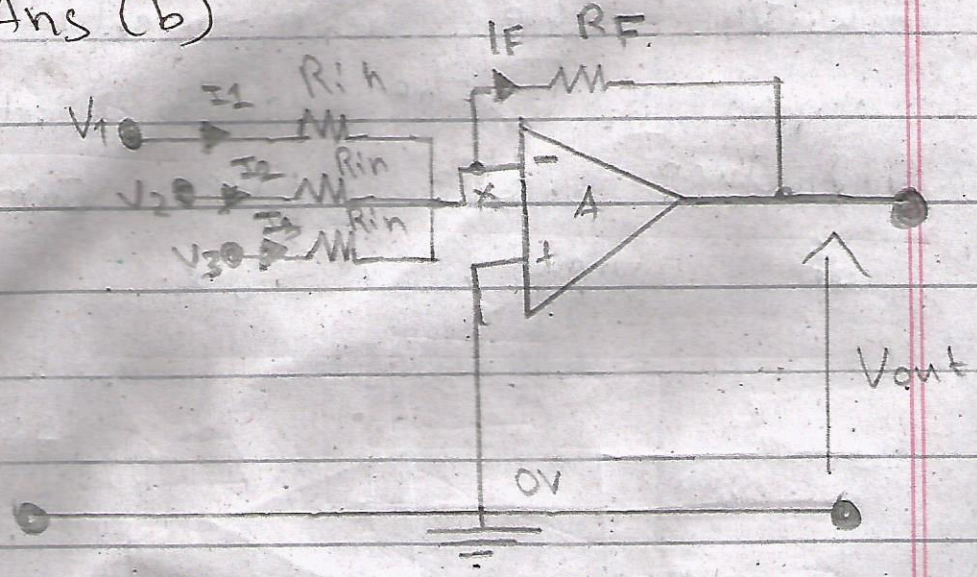


. An inversion of the output signal with respect to the input as it is 180° out of Phase

∴ This is due to the feed-back is -ive in value.

(b)	**State** the following statement as **True** or **False** and also give the reason for your answer: "The output of a summing amplifier is positive"	Marks 06 CLO 2

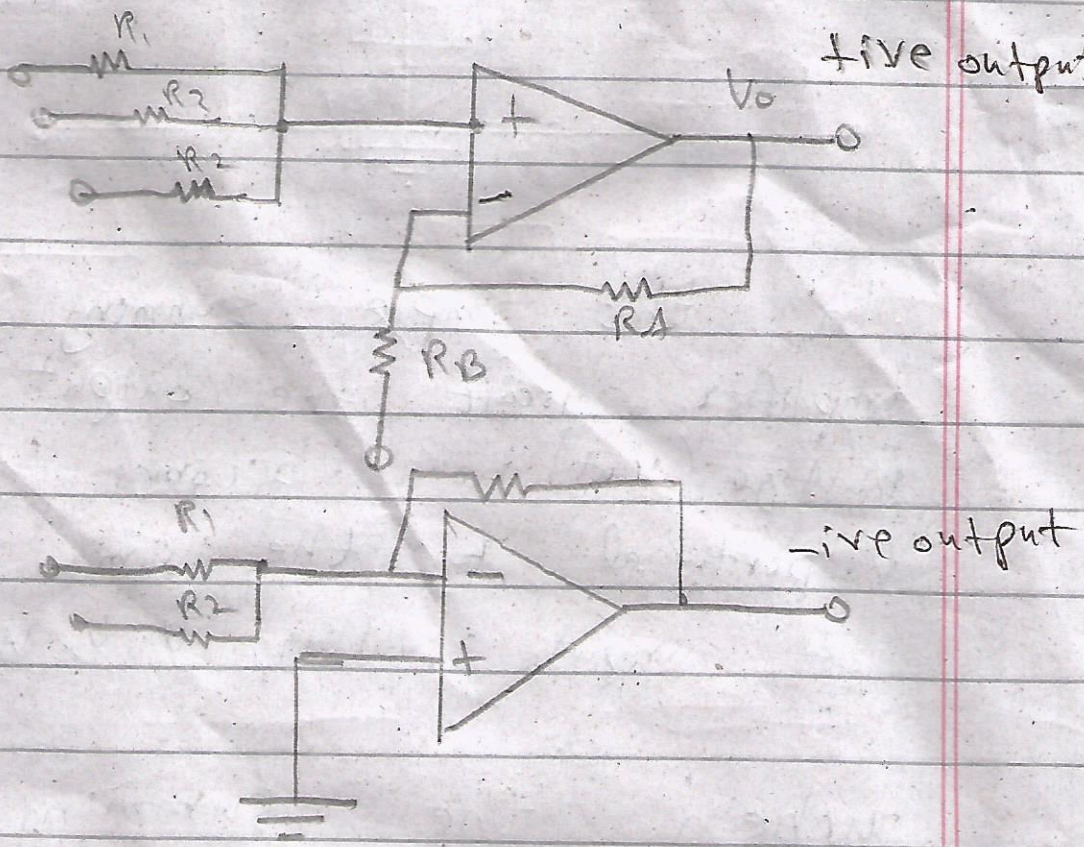
Ans (b)



"In this simple summing amplifier circuit, the output voltage (V_{out}) now becomes proportional to the sum of input voltages V_1, V_2, V_3"

When the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltage. or when the summing point is connect

with the non-inverting input of the op-amp it produce the tive sum of input voltages.



So The Answer is [redacted] also
True or Nor false