

NAME: SYED MUHAMMAD SHAH RIZVI
AD :: 14520
Semester :: 4th Spring 2020
Program : BSCS
Paper : Final
Subject : Computer Architecture

Q-NO-1(a)

Addressable Units::

In some systems, the addressable unit is the word. However, many systems allow addressing at the byte level. In any case, $2^d = N_a$.

UNIT OF TRANSFER::

For main memory this is the number of bits read out of or written into memory at a time. The unit of transfer need not equal a word or an addressable unit.

Word::

The "natural" unit of organization of memory. The size of a word is typically equal to the number of bits used to represent an integer and to the instruction length.

Q. No-1(b)

Replacement Algorithms..

A number of algorithms have been tried. We mention ~~four~~ of a most common. Probably the most effective is least recently used (LRU): Replace the longest with no reference to it. Still another possibility is least frequently used (LFU): Replace that block in the set that has experienced the fewest references. LFU could be implemented by associating a counter with each line.

Q-NO-1(c)

SRAM:

The SRAM address line is used to open or close a switch. The address line controls two transistors (T_5 and T_6). When a signal is applied for this line, the two transistors are switched on, allowing a read or write operation.

For a write operation, the desired bit value is applied to line B, while its complement is applied to line \bar{B} . This forces the four transistors (T_1, T_2, T_3, T_4) into the proper state. For a read operation, the bit value is read from line b.

Q-NO-1(d)

Discusses 16-Mbit DRAM (4Mx4) organization ~~very diagram.~~

DRAM:

is a type of random access semi-conductor memory that stores each bit of data in a memory cell consisting of a tiny capacitor and a transistor. Only 4 bits are read/written to this DRAM, there must be multiple DRAMS connected to the memory controller to read/write a word of data to the bus.

All the DRAMs require a refresh operation. A simple technique for refreshing is in effect to disable the DRAM.

Q-NO-1(e)

DVD's Capacity: Over CD ::

^{storage} data¹ is higher for a few interrelated reasons. ↓ DVD's

DVD uses a red, rather than infrared, laser. Red light has a shorter wavelength than infrared light.

DVD has a smaller numerical aperture than CD does.

Q-NO-2(a)

Ans EEPROM

- * EEPROM uses NOR type memory.
- * EEPROMs are seldom rewritten
- * EEPROM is used when only small amounts are needed
- * EEPROM is a type of memory devices that uses an electronic device to erase or write digital data.

Flash Memory ::

- * Flash is just one type of EEPROM
- * Flash uses NAND-type memory
- * Flash is block-wise erasable
- * Flash is constantly rewritten
- * Flash is used when large amounts are needed.

Q-NO-2(b)

HARD FAILURE ::

Hard failures are errors that occur through process defects or circuit bugs. Hard failures are repeatable with the correct sequence of actions within the microcontroller.

Soft ERRORS ::

Soft errors occurs through no failure of the circuit or defect but due to an external source that causes data to change.

Q.NO-2(c)

Magnetic Disk ::

A magnetic disk is a storage device that uses a magnetization process to read, write, rewrite and access data.

Q.NO-2(d)

Parallel Access and Independent Access RAID Schemes ::

In parallel access, all the disks are accessed at once, whereas in independent access, the disks run independently of each other.

Q.NO-2(e)

HD DVD and Blu-ray DVD ::

HD DVD players have been much cheaper than Blu-ray machines, but Blu-ray discs have

more storage and more advanced protections against piracy. Both versions deliver sharp resolutions.

Q-No-3(a)

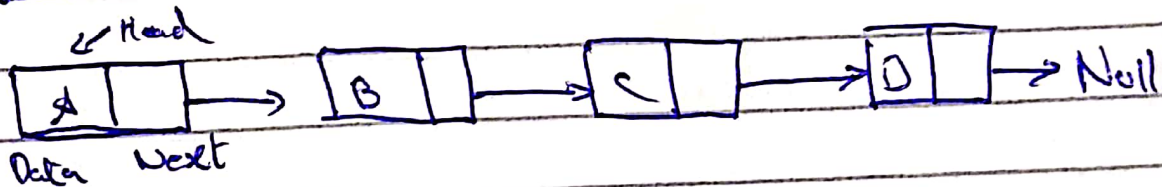
MEMORY Access Methods:

These are

4 types of memory access.

1) Sequential Access:

In this method, the memory is accessed in a specific linear sequential manner, like accessing in a single linked list.



(ii) Random Access:

In this method, any location of the memory can be accessed randomly like accessing in array. Physical locations are independent in this access method.

(iii) Direct Access:

In the method, the particular location of the memory can be accessed directly like accessing in array.

iv) Associate Access ::

In this memory, a word is accessed rather than its address. This access method is special type of random access method.

Q. NO - 3(b)

PRINCIPAL OF Locality ::

Reference also known as the ^{locality of} principle of locality, the phenomenon of the same value or related storage locations being frequently accessed. Locality occurs in time (temporal locality) and in space (Spatial locality).

• TEMPORA Locality ::

refers to the reuse of specific data or resources.

• Spatial Locality ::

refers to the use of data elements within relatively close storage locations.

Q-NO-3(c)

Cache Coherence:

In computer architecture, cache coherence is the uniformity of shared resource data that ends up stored in multiple local caches. When clients in a system maintain caches of a common memory resources, problems may arise with incoherent data, which is particularly the case with CPUs in a multiprocessing system.

Q-NO-3(d)

Practical Issues Peculiar to SSDs.

- SSD performance has a tendency to slow down as the device is used.
- The entire block must be read from the flash memory and placed in a RAM buffer.
- Before the block can be written back to flash memory, the entire block of flash memory must be erased.
- The entire block from the buffer is now written back to flash memory.

Q-NO-3(e)

CD Read and Write Operation..

CD-RW (Compact Disc-Rewritable) is a digital optical disc storage format introduced in 1997. Unlike CD-ROM Compact Discs (CD-ROMs) can be written, read, erased and re-written.

CD-RWs, as opposed to CDs, require specialized readers that have sensitive laser optics. Consequently, CD-RWs cannot be read in many CD readers built prior to the introduction of CD-RW.

Q-No-4(a)

Ans... In our example

Suppose 95% of the memory access are found in level 1. Then average time to access a word can be expressed as.

$$(0.95)(0.01 \mu s) + (0.05)(0.01 \mu s + 0.1 \mu s) =$$
$$0.0095 + 0.0055 = 0.015 \mu s$$

The average access time is much closer to 0.01 μs than to 0.1 μs , as derived.

Q. No - 4(b)

$$\text{Total block in the cache} = \frac{8 \text{ kbytes}}{16 \text{ bytes}} \\ = 2^7 \times 2^{10} / 2^4 = 2^9 = 512$$

Number of set = number of block in cache / 2

$$\text{Number of set} = 512 / 2$$

$$\text{Number of set in cache} = 256$$

$$\text{Number of set in cache} = 2^8$$

$$\text{Number of set} = 8$$

$$\text{Size of block} = 16 = 2^4$$

$$\text{Size of memory} = 2^6 \times 2^{20} = 2^6$$

$$\text{Tag} = \text{size of memory} - \text{size of block}$$

$$\text{Tag} = 26 - 8 - 4$$

$$\text{Tag} = 14$$

tag	set	Size of block
14	8	4

Q. No - 4(c)

Ans ::

Sol ::

$$M = 8$$

$$2^k - 1 \geq k + m$$

$$2^4 - 1 \geq 4 + 8$$

$$15 \geq 12$$

1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	1	1	0	0	1	0	0	1	0

The check bits are in a bit numbers
1, 2, 4 & 8

check bit 8 calculated by values in bit
numbers 9, 10, 11, and 12.

check bit 4 calculated by values in bit
numbers 5, 6, 7 and 12.

check bit 2 calculated by values in bit
numbers 3, 6, 7, 10 and 11.

check bit 1 calculated by values in bit
numbers 3, 5, 7, 9, 10 and 11.

Thus, the check bits are left.

Q-NO-4(d)

Sol:-

7200 revolution in 60 sec

1 revolution in $60/7200$ sec

1 revolution in 6ms

1 revolution: Covering one entire track = 500 sectors

500 sectors = 6ms

1 sector = 8 microsecond

Now there are 2 different things

(i) 2500 sectors so time = $2500 \times 8 \text{ms} = 20 \text{ms}$

(ii) 1.28 MB = 1342177028 Bytes or
2621.44 sectors = 2622 sectors = 20.976ms

Total time case:

Case (i) $4 + 2 + 20 = 26 \text{ms}$

Case (ii) $4 + 2 + 20.976 = 26.976 \text{ms}$