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Reg# 16549

Semester 6th

Assignment: DLD Lab

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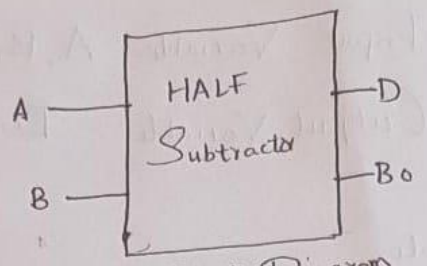
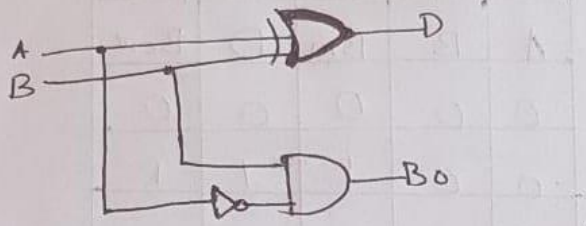
Lab 4: HALF Subtractor



Block Diagram



Logic Circuit of Half Subtractor

Table 4.1:

Inputs		Outputs	
A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Lab - 4

4.7 Observation Table

Full Subtractor- Input Variable - A, B, BIN

Output Variable :- D, B out

Table

Inputs			Outputs	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1