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1) What is the general relationship among access time, memory cost, and capacity?
As access time becomes faster, the cost per bit increase, As memory size increases the cost per bit is smaller Also, with greater capacity, the access time becomes slower.

2) Discuss different memory access method in detail?
Another distinction among memory types is the method of accessing units of data. These include the following:

- Sequential access:-
  Memory is organized into units of data, called records. Access must be made in a specific linear sequence. Stored addressing information is used to separate records and assist in the retrival process. A shared read write mechanism is used and this must be moved from its current location to the desired location, passing and rejecting each intermediate record. Thus the time to access an arbitary record is highly variable.
- Direct access:-
  As with sequential access direct access involves a shared read write mechanism is used, and this

must be moved from its current location to the desired location, passing and rejecting each inter-mediate record. Thus, the time to access an arbitary record is highly variable.

Random access:

Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant, thus any location can be selected at random and directly addressed and accessed. Main memory and some cache systems are random access.

Associative:

This is a random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, and to do this for all words simultaneously. Thus, a word is retrieved based on a portion of its contents rather than its address.

Discuss the importance of memory hierarchy?

Memory hierarchy is particularly important for understanding optimizations and performance costs that happen at the hardware level. Storing data on disk

versus main memory can impact running time. the structure of page tables virtual memory and lookup caches also play a significant role.

(5) V:-

Direct mapping:

It is the simplest technique.

- Maps each block of main memory into only one possible cache line.

Associative mapping:

- permits each main memory block to be loaded into any line of the cache.
- The cache control logic interprets a memory address simply as a tag and a word field.
- To determine whether a block is in the cache, the cache control logic must simultaneously examine every line's tag for a match.

Self associative mapping:

A compromise that exhibits the strengths of both the direct and associative approaches while reducing their disadvantages.

Q2 Write note each on the following:

① Memory Unit of transfer:

It is the maximum no of bits that can be read or written into the memory at a time. In case of main memory it is mostly equal to

word size, In case of external memory, unit of transfer is not limited to the word size. It is often larger and is referred to as blocks.

" Memory performance parameters:
- Access time (latency):
- Memory cycle time.
- Transfer rate.

The two most important characteristics of memory and capacity and performance the above 3 performance parameters are used.

(iii) Disk cashe:
- A portion of main memory can be used as a buffer to hold data temporarily that is to be read out to disk.
- A few large transfers of data can be used instead of many small transfers of data.
- Data can be retrieved rapidly from the software cashe rather than slowly from the disk.

(iv) Replacement algorithms:-

Once the cashe has been filled, when a new block is brought into the cashe, one of the existing blocks must be replaced. For direct mapping, there is one possible line for any particular block and no choice is possible, for the associative and set-associative techniques a replacement algorithm is needed, to achieve high speed, such as algorithm must be implemented in hardware.

(5) possible approaches to cashe memory:
possible approaches to cashe coherency include the following:

- Bus watching with write through.
- Hardware transparency
- Non-cacheable memory

(6) logical cashe:-

Also known as virtual cache stores data using virtual addresses.

physical cashe.

A physical cashe stores data using main memory physical addresses.

Q3 Diff each of the following:

(1) Sequential access:

Memory is organized into units of data called records. Access must be made in a specific linear sequence. Stored addressing info is used to separate record and assist in the retreival process.

(2) Direct access:-

It involves a shared read-write mechanism. Access is accomplished by direct access to reach a general vicinity plus sequential searching counting or waiting to reach the final location.

Random acces:

Each addressable location in memory has a Unique physically wired in addressing mechanism. The time to access a given location is independant of the sequence of prior accesses and is constant.

(2) Direct mapping:

Simple and inexpensive to implement its main disadvantage is that there is fixed cache location for any given block.

(i) Associative mapping:

With associative mapping, there is flexibility as to which block to replace when a new block is read into the cache.

(ii) set associative mapping:

Set associative mapping is a compromise that exhibits the strengths of both the direct and associative approaches while reducing their disadvantages.

(3) Split cache:

- Has become common to split cache
- one dedicated to instructions
- " " " data

Trend is toward split cache at the L1 and Unified caches for higher levels.

Unified cashe:

- Trend is toward unified cashes for higher levels.
- Higher hit rate.
- Only one cashe needs to be designed and implemented.

Q4 write through

- Simplest technique.
- All write operations are made to main memory as well as to the cashe.

write back:

Minimizes memory writes.
Updates are made only in the cashe
This makes for complex circuitry and a potential bottle neck.