DLD Assignment final

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Submitted To:
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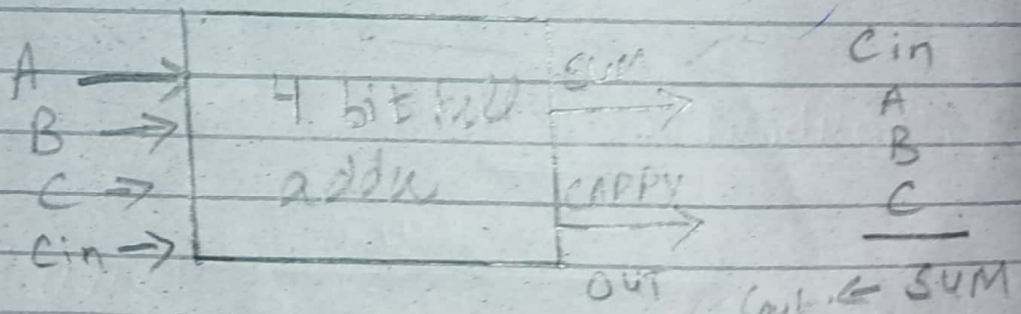
Q1) Draw and explain logic diagram for each of following.

A) A circuit for adding or subtracting two 4 bit numbers

4bit

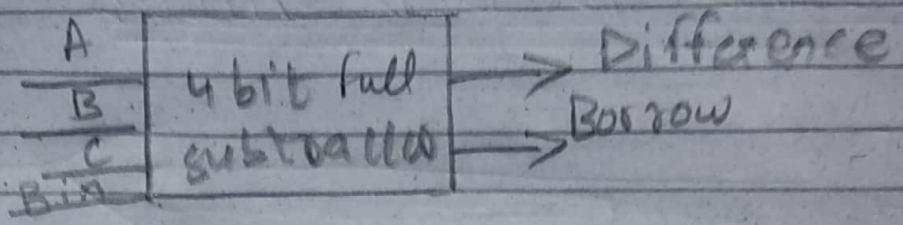
1) Full adder:

The full adder is logical circuit, that Perform an addition operation on three binary digits, and just like an half adder, it also generate carry. In many ways full adder can be used as half adders connected together.

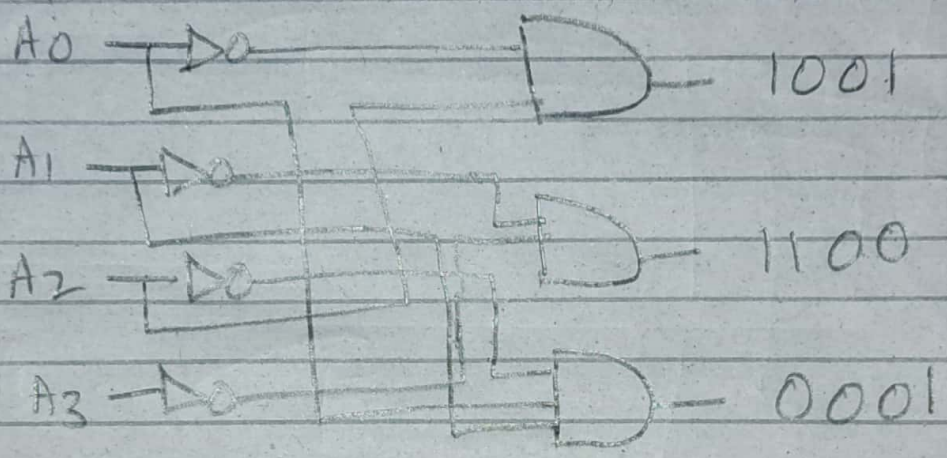


b) 4 bit full subtractor:

The 4 bit full subtractor is logical circuit, that perform subtraction operation on three binary digits, and just like an half subtractor, it also generate Borrow In many ways full subtractor can be used as half subtractors connected together.

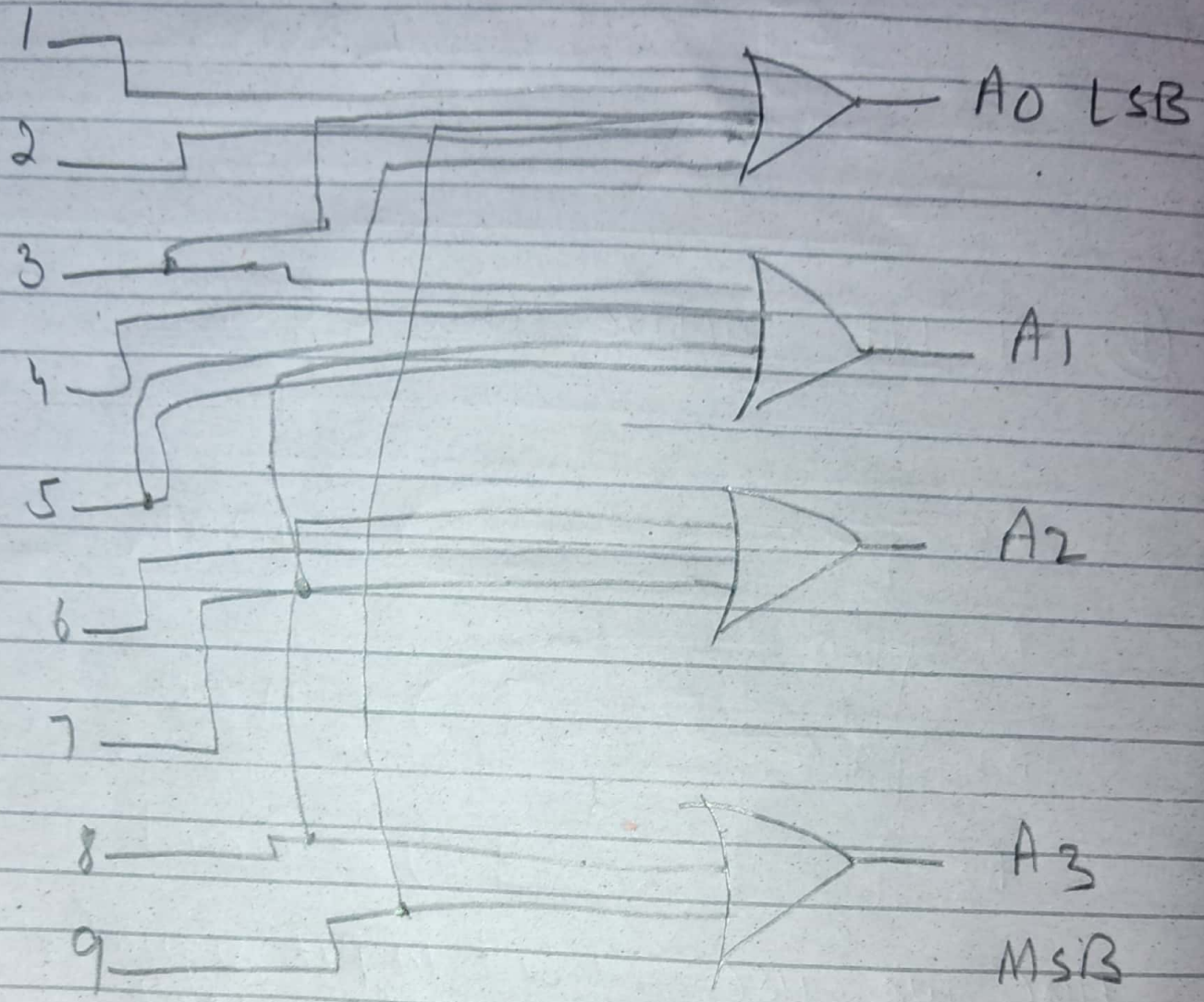


(5) 4 bit active low decoder:



Here, we use 4 bit input signal A and it detect the value 1001.
The active low decoder means that output is active it has logic value, which is low, rather than logic value high. This decoder works as active low enable input is high.

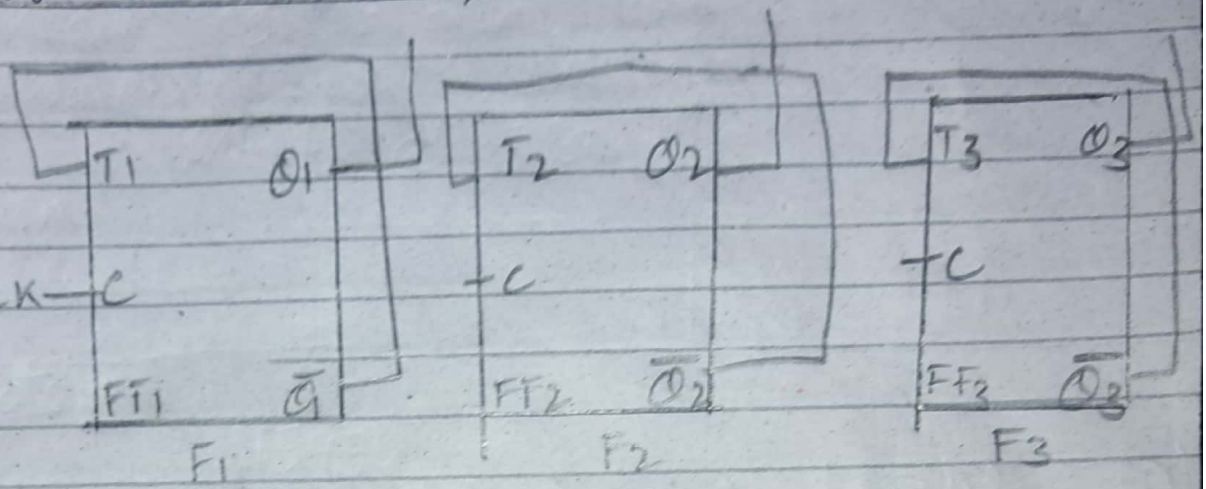
(c) Decimal to BCD encoder:



A decimal to BCD encoder is also known as 10 line to 4-line encoder, it accepts 10 input and product 4bit output corresponding to activated decimal input.

(4)

(d) Frequency divider (use 3 J-K flip flop and assume 16 KHZ frequency as initial wave form).



Here we assume the frequency is 16 KHZ.

So f/2, f = 16/2

f = 8 KHZ.

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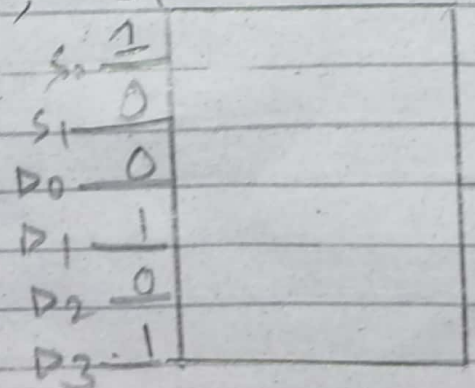
(02) for 4 input multiplexer, data inputs are given as

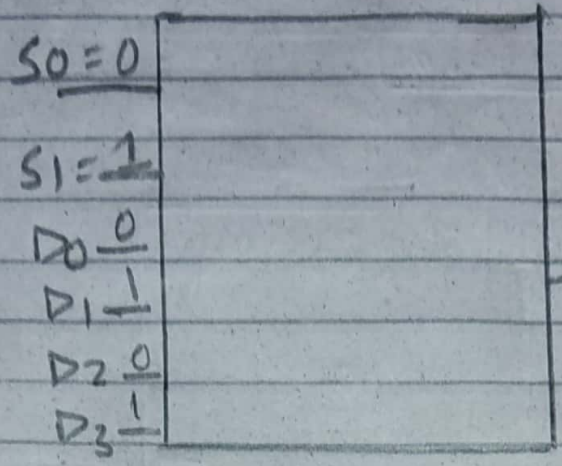
D0 = 0, D1 = 1, D2 = 0, D3 = 1, find output Y, if select input are

(a) S0 = 1, S1 = 0.



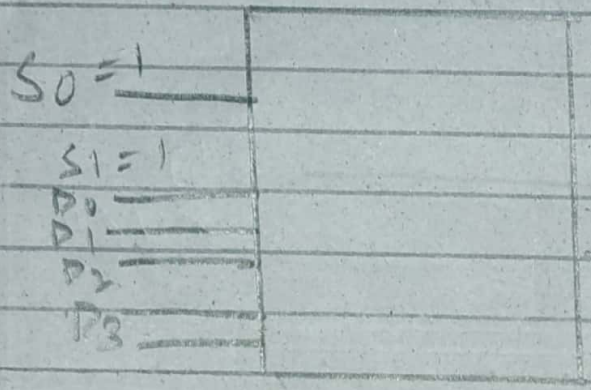
(5)

(b) $S_0 = 0$, $S_1 = 1$



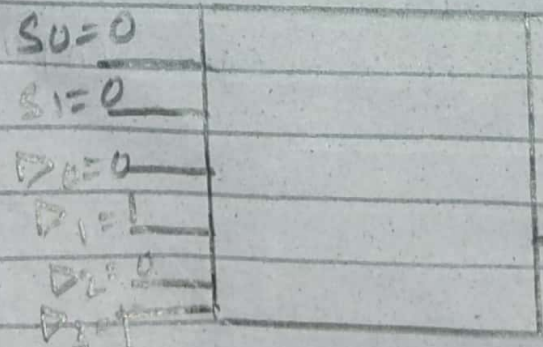
$S_0 \cdot S_1 = D_1$
$0 \cdot 1$

(c) $S_0 = 1$, $S_1 = 1$



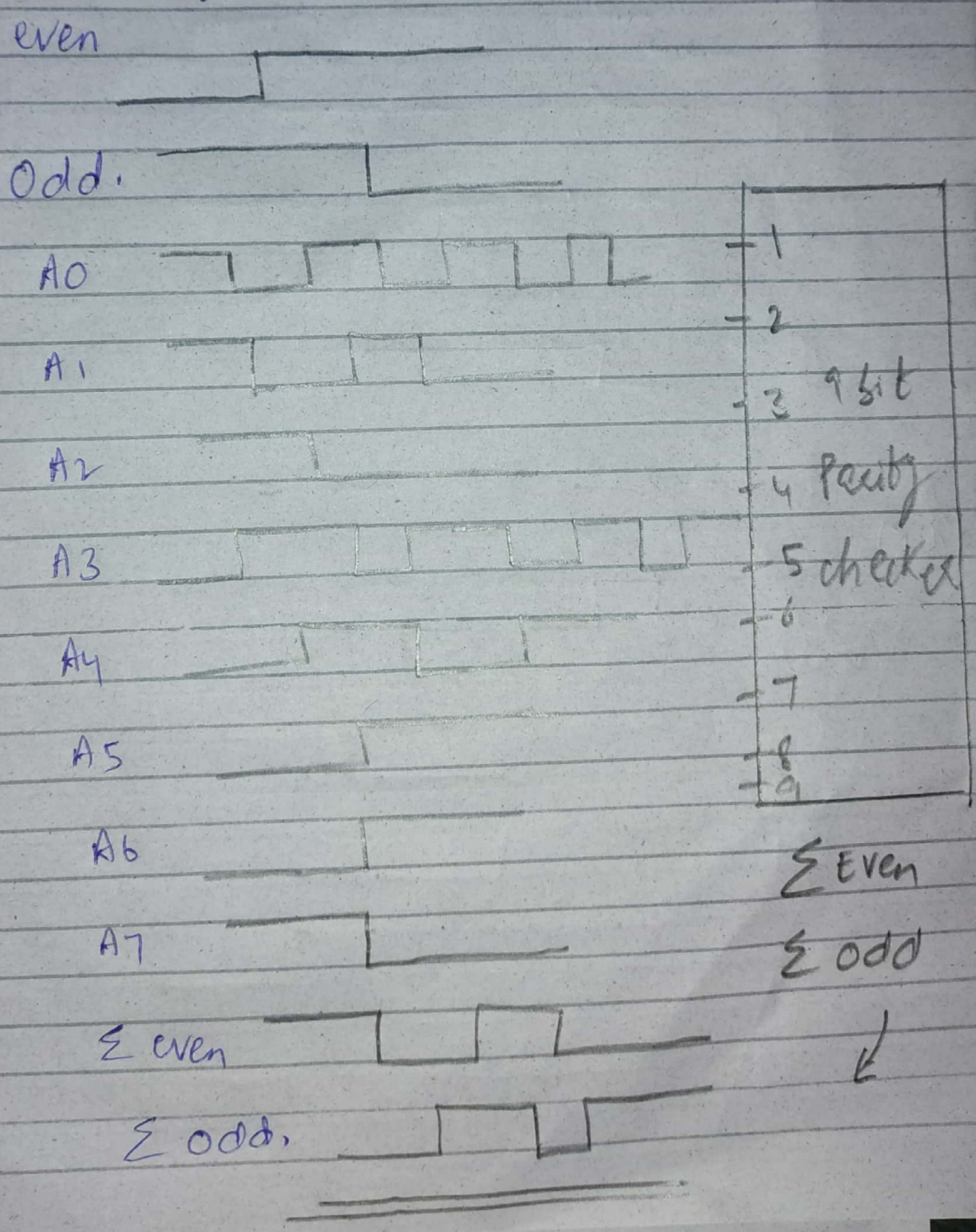
$S_0 \cdot S_1 = D_2$
$1 \cdot 0$

(d) $S_0 = 0$, $S_1 = 0$.

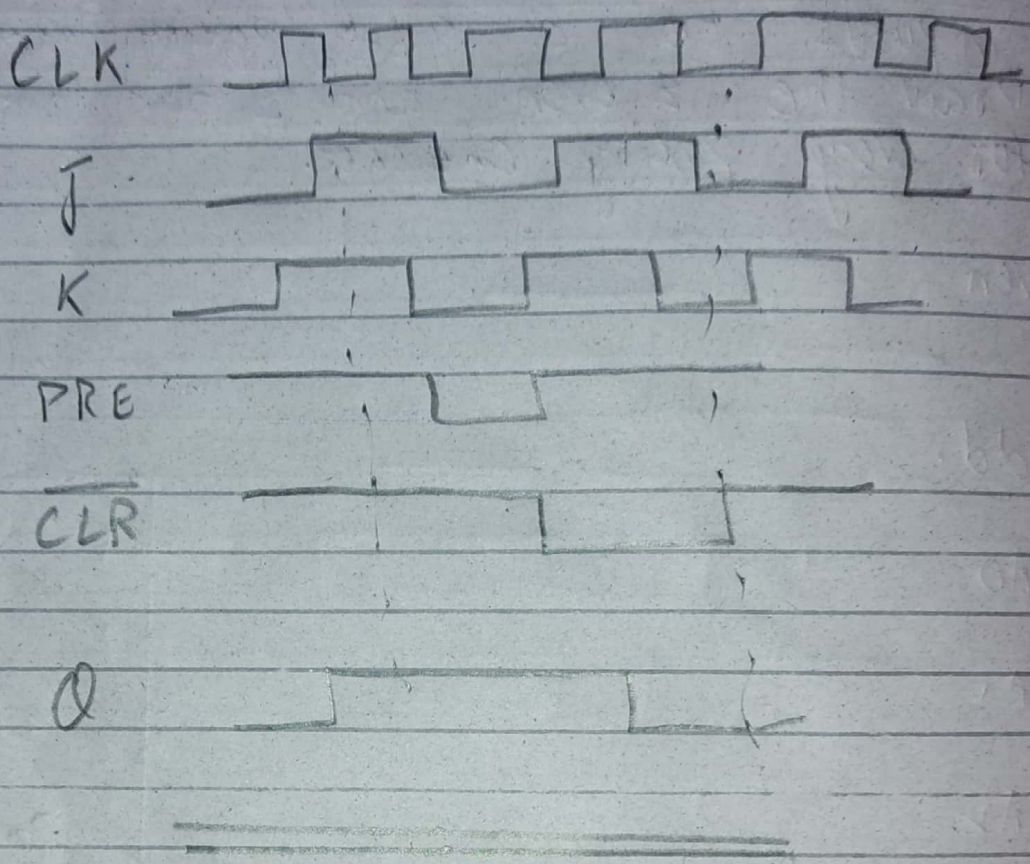


$S_0 \cdot S_1 = D_3$
$1 \cdot 1$

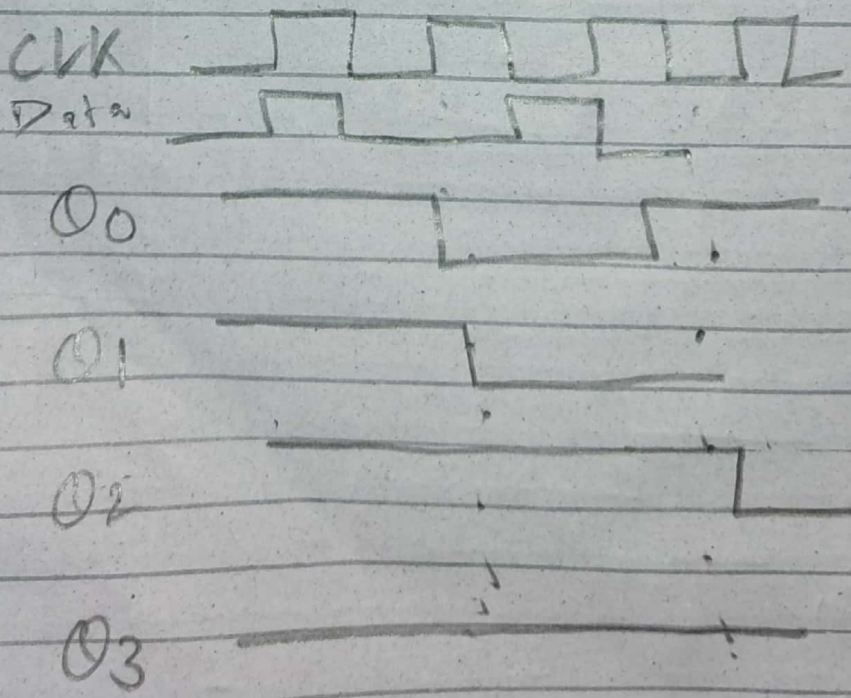
(03) Timing diagram in figure 01 shows inputs to a 9 bit parity checker. Draw the Σ even and Σ odd, output for every parity checker.



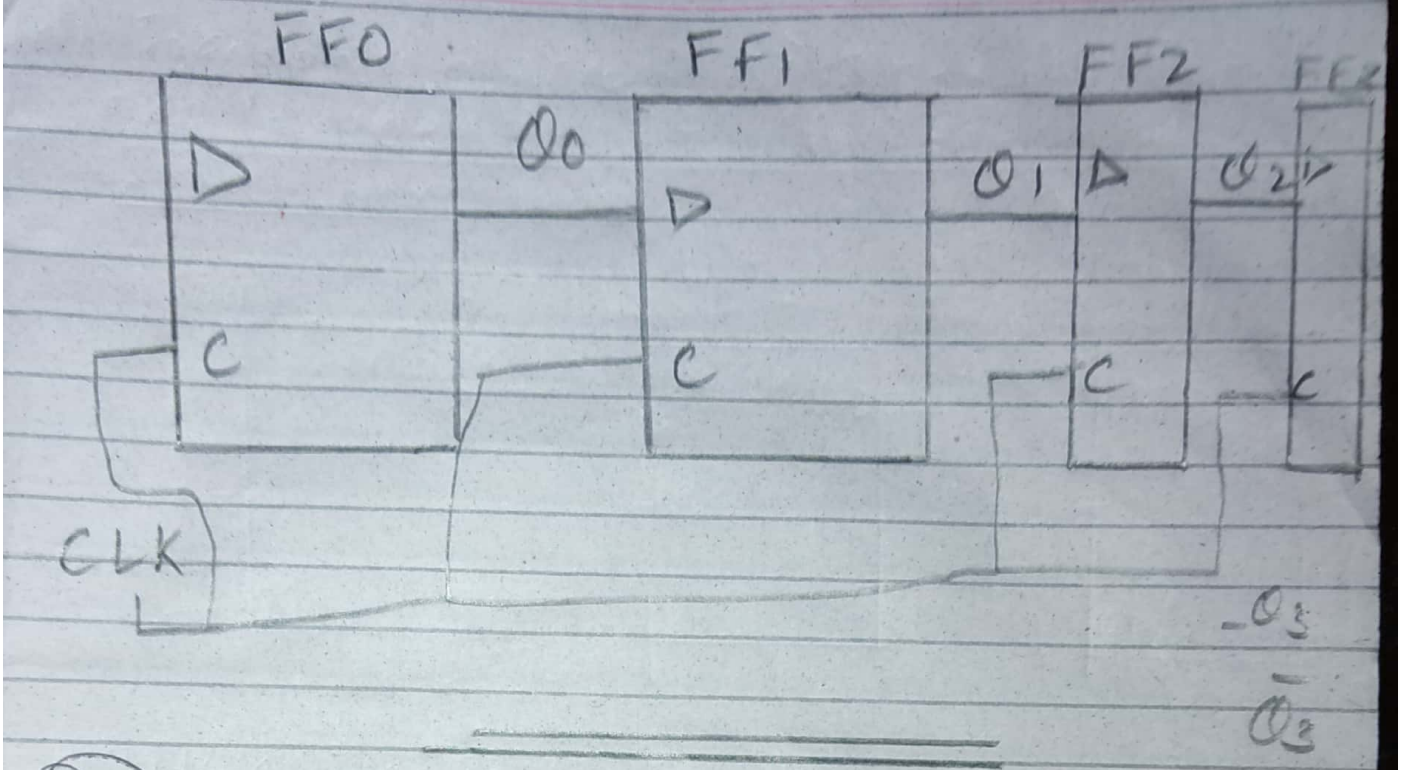
Q4



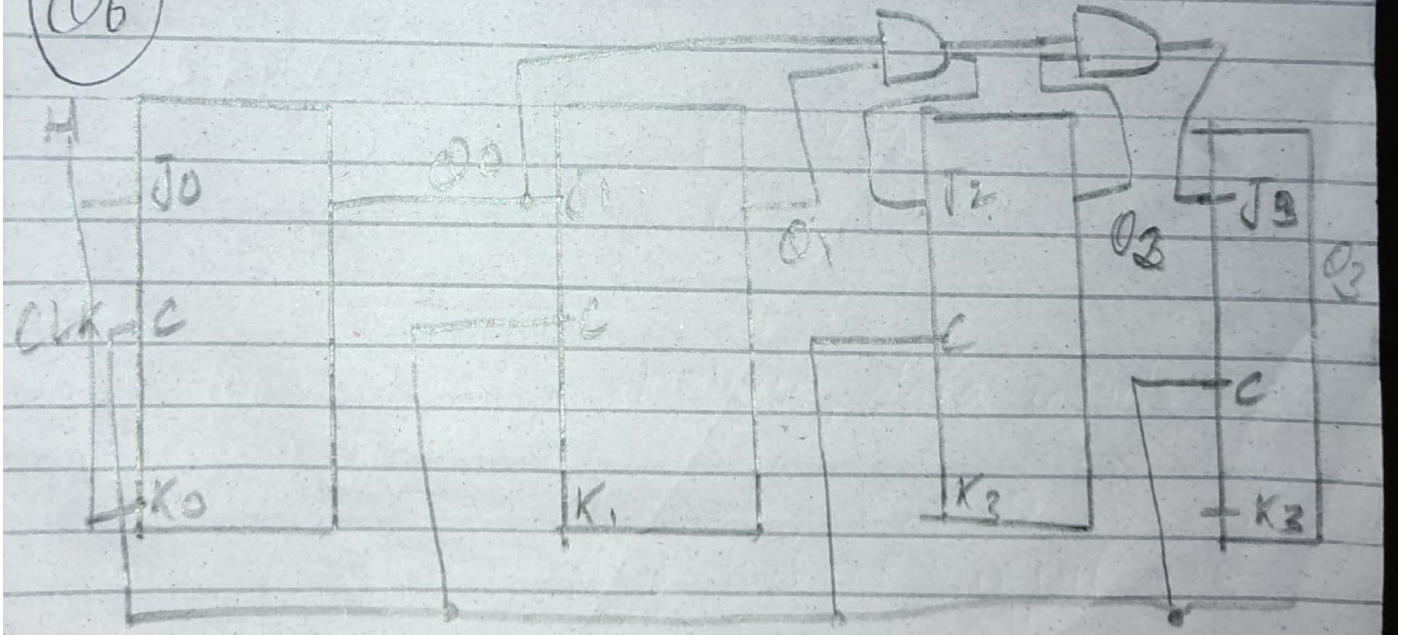
Q5



(8)



(6)



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