ID # 13794 ASSIGNMENT # 2

Muhammad Zarak Khan Digital Logic Design

Q3 a) The waveform in the figure 01 shows input to a 4-bit parity checker. Draw the E even & E odd for the even parity checking.

Ans:

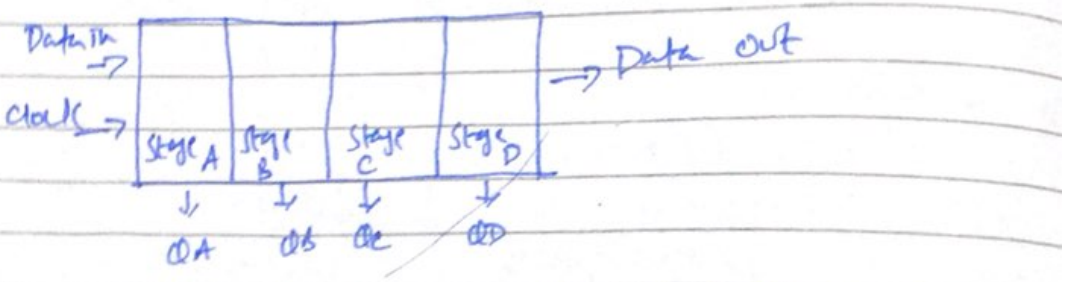
Clock Reference data

Symbol	Parameter	Condition	Typical	
			HC	HCT
t_{PLH}/t_{PHL}	propagation delay I_n to E_V	$C_L = 15pF, V_{CC} = 5V$	17	18
	I_n to E_O		20	22
C_I	Input Capacitance		5.5	3.5
C_{PD}	Power dissipation capacitance per package		65	65

Q5) Use the waveforms in figure 05 to draw the timing diagram for the parallel outputs

Ans: Using Serial-in, parallel out Shift register.

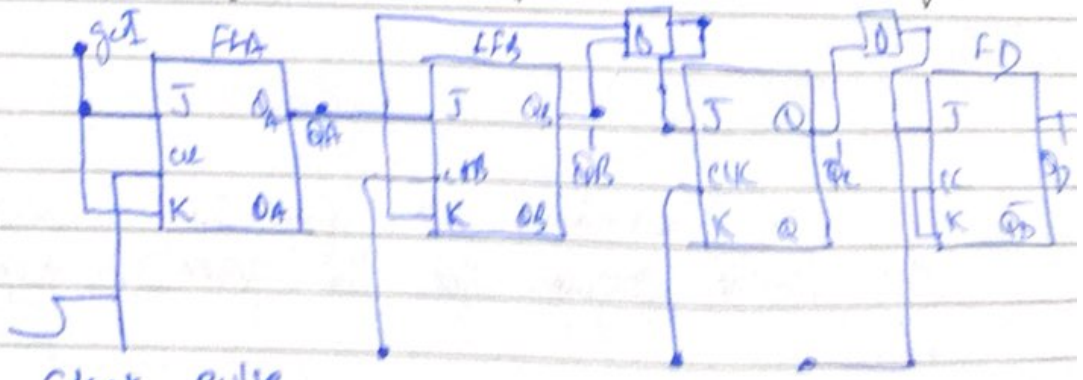
If four data bits are shifted in by four clocks via a single wire at data-in, below the data becomes available simultaneously on the four outputs Q_A to Q_D after the fourth pulse

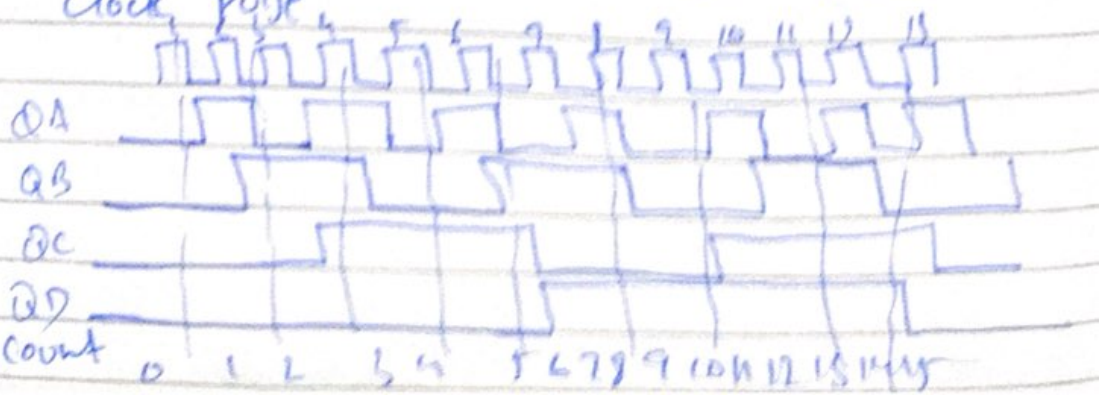


Serial-in parallel out shift register with 4 stages

(06) Draw the logic diagram & timing diagram for the 4 bit stage synchronous binary counter

Ans:

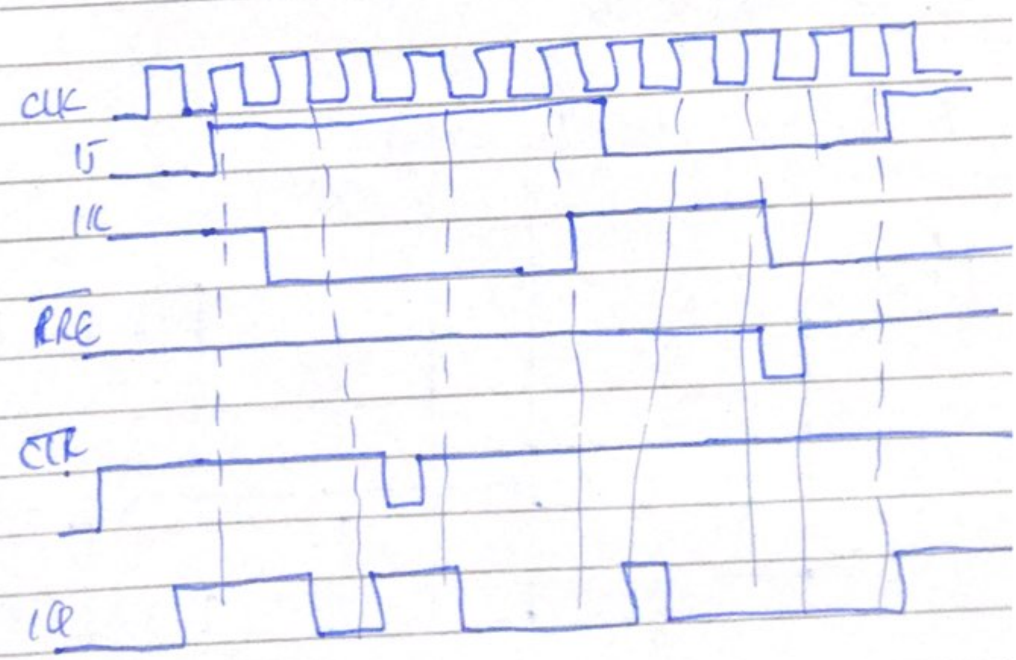




Q4) ~~The waveforms in figure are shown applied to~~ ~~...~~
The waveform in figure ~~shows~~ are applied to the J, K, CLK, $\overline{PRE}$, & $\overline{CLR}$ inputs as indicated. Determine the Q output, if the flip-flop is initially RESET

Ans Lets look at the two specific edge-triggered flip-flops. The are representative of the various types & of flip-flops available in fixed-function IC form & like most other devices.
Also we learn how VHDL is used to describe the types of flip flops.

ex The 1J, 1K, 1CLK, 1PRE & 1CLR waveforms in figure 7 - are applied



The resulting IQ waveform is shown in fig 7. Note that each time a LOW is applied to the $\overline{CLR}$ to CLR the flip-flop is set or reset regardless the state of the other inputs.

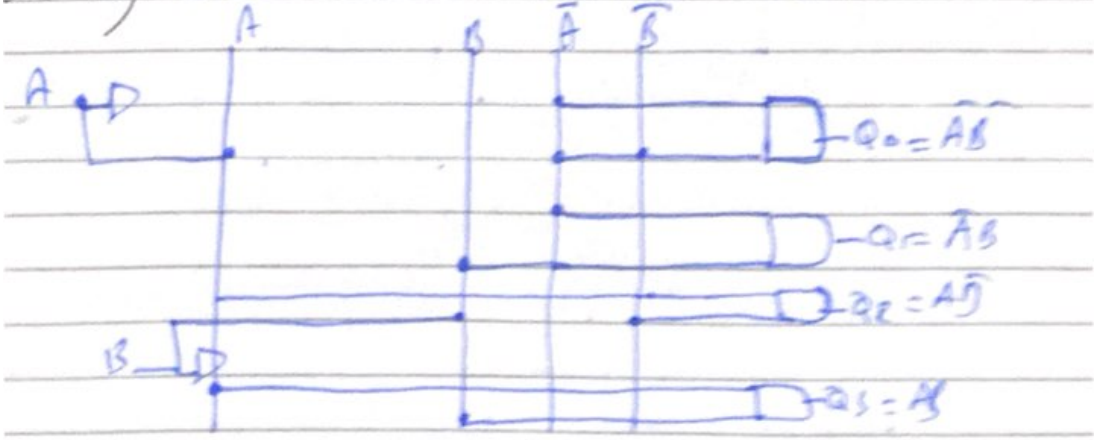
Q1) Draw & explain the logic diagram for each of the following.

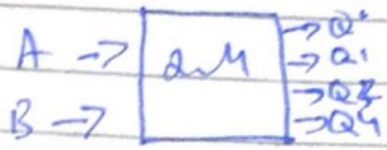
a) A circuit for adding or substracting two 4 bit numbers

SOL: Parallel Adder/Substractor

The operation of both adding & Substraction can be performed by a one common binary adder. Such binary circuit can be designed by adding an Ex-OR gate with each full adder by shown. The mode input Control line M is connected with carry input of the least significant bit of the full adder.

21 B) 4 bit active low decoder





A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Q1 c

Sol: $(345)_{10} = (?)_{BCD}$

$\frac{3}{0011}$ $\frac{4}{0100}$ $\frac{5}{0101}$

$(0011\ 0100\ 0101)$

$(345)_{10} = (0011\ 0100\ 0101)_{BCD}$