Assignment: 3

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Q.1 Give answer to each of the following.

Ans: A

Two approaches can be taken to dealing with multiple interrupts.

The first is to disable interrupts while an interrupt is being processed.
A disable interrupt simply means that the processor can and will ignore that interrupt request signal. if an interrupt occurs during this time, it generally remains pending and will be checked by the processor after the processor has enabled interrupts.

The second approach is to define priorities for interrupts and to allow an interrupts and to allow an interrupt of higher priority to cause a lower-priority interrupt handler to be itself interrupted. As an example of this second approach, consider a system with three I/O devices, a printer a disk, and a communication line with increasing priorities of 2, 4, and 5 respectively.

Ans: B

Memory: Typically, a memory module will consist of N word of equal length. Each word is assigned a unique numerical address (0, 1, ..., N-1). A word of data can be read from or written into the memory. The nature of the operation is indicated by read and write control signals.

I/O module: from an internal (to the computer system) point of view, I/O is functionally similar to memory. There are two operations: read and write. Further, an I/O module may control more than one external device. We can refer to each of the interfaces to an external devices as a port and give each a unique address (e.g., 0, 1, ..., M-1).

Processor: The processor reads in instruction and data, writes out data after processor, and uses control signals to the overall operation of the system. it also receives interrupt signals.

Ans: C

QPI Protocal Layer: In this layer, the packet is defined as the unit of transfer. The packet contents definition is standardized with some flexibility allowed to meet differing market segment requirements. A typical data packet payload is a block of data being sent to or from a cache.

Ans: D

PCI Physical and Logical Architecture.

A root Complex device, also referred to as a chipset or a host bridge. Connects the processor and memory subsystems to the PCI Express switch fabric comprising one or more PCIe and

PCIe switch devices.

* Switch: The switch manages multiple PCIe streams.

* PCIe endpoint: An I/O device or controller that implements PCIe such as a Gigabit ethernet switch, a graphics or video controller, disk interface, or a communications controller.

Legacy endpoint: legacy endpoint category is intended for existing design that have been migrated to PCI Express endpoints are not permitted to require the use of I/O space at runtime and must not use locked transactions.

Q.2 Write short note on each of the following:

Ans: A

instruction cycle. The processing required for a single instruction is called an instruction cycle. Using the simplified two-step description given. The two steps are referred to as the fetch cycle and the execute cycle. Program execution halts only if the machine is turned off, some sort of unrecoverable error occurs. On succeeding instruction cycles it will fetch instructions from locations 301, 302, 303 and so on.

Ans: B

Instruction Cycle State Diagram.

1: Intruction fetch: (if): Read instruction from its memory location into the Processor.

2: Intruction operation decoding (iod) Analyze instruction to determine type of operation to be performed and operand to be used.

3: Operand address Calculation: (oac): if the operation involves reference to an operand in memory or available via I/O then determine the address of the operand.

4: operand fatch: (of): fetch the operand from memory or read it in from I/O

5: Data operation: (do): Perform the operation indicated in the instruction.

6: Operand store (~~do~~os) write the result into memory or out to I/O

Ans: C

Classes of Interrupts:

Program: Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.

Timer: generated by a timer within the processor. This allows the operating system to perform certain functions on a regular basis.

I/O: generated by an I/o controller to signal normal completion of an operation, request service from the processor.

Hardware failure: generated by a failure such as power failure or memory Parity error.

Ans: D

Bus interconnection Scheme:

Data lines: The data lines provide a path for moving data among system modules. These lines, collectively, are called the data bus. The data bus may consist of 32, 64, 128 or even more separate lines the number of line being referred to as the width of the data bus.

Address lines: are used to designate the source or destination of the data on the data bus. for example, if the processor wishes to read a word (8, 16, or 32 bits) of data from memory, it puts the address of the desired word on the address lines. Clearly, the width of the address bus determine the maximum possible memory capacity of the system.

Control lines: are used to control the access to and the use of the data and address lines

Because the data and address lines are shared by all components there must be a mean

of controlling their use.

Q.3 Differentiate each of the following.

Ans: A

Hardware a segment that can accept a cod and generate control signals. Instead of rewiring the hardware for each new pro gram, all we need to do is provide anew sequence of codes. Each code is, in effe ct, an instruction, and part of the hard- ware interprets each instruction and generates control signals.

Programming in Software: To distinguish this new method of programming, a sequence of codes or instructions is called Software software indicates two majo components of the system: an instru ction interpreter and a module of general-purpose arithmetic and log functions. These two constitute the CPU.

Ans: B

We have a User Program that contains two WRITE Commands. There is a segment of Code at the beginning then on WRITE Command. then a second segment of Code, then a second WRITE Command. then a third and final segment of Code. The WRITE Command invokes the I/O Program provided by the OS. Similarly, the I/O program consists of a segment of code followed by an I/O command followed by another segment of Code.

Q.4 Solve each of the following:

Ans: A

	Memory
300	3005
301	5940
302	7006
.	
.	
940	0002
941	

We will assume that the memory (contents in hex) as the previous table:

300: 3005; 301 5940; 302: 7006

Therefore, the steps will be as the following:

step 1: 3005 → IR

step 2: 3 → AC

step 3: 5940 → IR

step 4: 3+2=5 → AC

step 5: 7006 → IR

step 6: AC → Device 6

Ans: B

Step 1: The PC contains 300, the address of the first instruction. This value is loaded in to the MAR. The value in location 300 is loaded into the MBR, and the PC is incremented These steps can be done in parallel. The value in the MBR is loaded into the IR.

Step 2: The address Portion of the IR (940) is loaded into the MAR. The value in location 840 is loaded into the MAR.
The value in the MBR is loaded into the MAR

Step 3: The value in the PC (301) is loaded in to the MAR. The value in location 301 is loaded into the MBR, and the PC is incremented. The value in MBR is loaded into the IR.

Step 4: The address Portion of the IR (941) is loaded into the ~~MBR~~ MAR
The value in the MBR is loaded into the MBR.

Step 5: The value in PC (302) is loaded in to the MAR The value in the MBR is loaded into the IR

Step 6: The address Portion of the IR (941) is loaded into the MAR.

The value in the AC is loaded into the MAR. The value in the MBR is stored in location 941.

Ans: C

a. 2^(32-8) = 2^24 = 16,777,216 bytes = 16MB, (8bits = 1 byte for the opcode).

b.1: a 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data.

b.2: a 16-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take four bus cycle each, two for the address and two for the data

C. for the PC needs 24 bits (24-bit addresses), and for the IR needs 32 bits (32-bit addresses).

Ans: D

Since minimum bus cycle duration = 4 clock cycles and bus clock = 8 MHz

Then, maximum bus cycle = 8M/4 = 2M/s

Data transferred per bus cycle = 16 bit = 2 bytes

Data transfer rate per second = bus cycle rate * data per bus cycle = 2M * 2 = 4 Mbytes

To increase its Performance

$$\text{Clock} = \frac{1}{\text{Frequency}} = \frac{1}{8\text{Mhz}}$$

$$= 125\text{ns}$$

one Bus cycle = 4x clock cycle =

$$4 \times 125\text{ns} = 500\text{ns}$$

Ans: E

a. Through a single bus cycle the 8 bit microprocessor tranfers one byte while 16 microprocessor transfers two byte

The 16-bit microprocessor has twice the data transfer rate

b. By assuming that we have to perform 50 transfers of operand and instruction which 25 are one byte long and 25 are two bytes long.

The 8-bit microprocessor needs $25 \times (2 \times 25) = 75$ bus cycle for the transfer.

The 16-bit microprocessor needs $25 + 25 = 50$ bus cycles.

Therefore, the data transfer rates differ by a factor of 1.5.